

DR2 17.3" Schematics Document

uFCPGA Mobile Penryn

Intel Cantiga-GM + ICH9M

2009-03-16

REV : X01

DY : Nopop Component

<Core Design>



Wistron Corporation
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Document Number

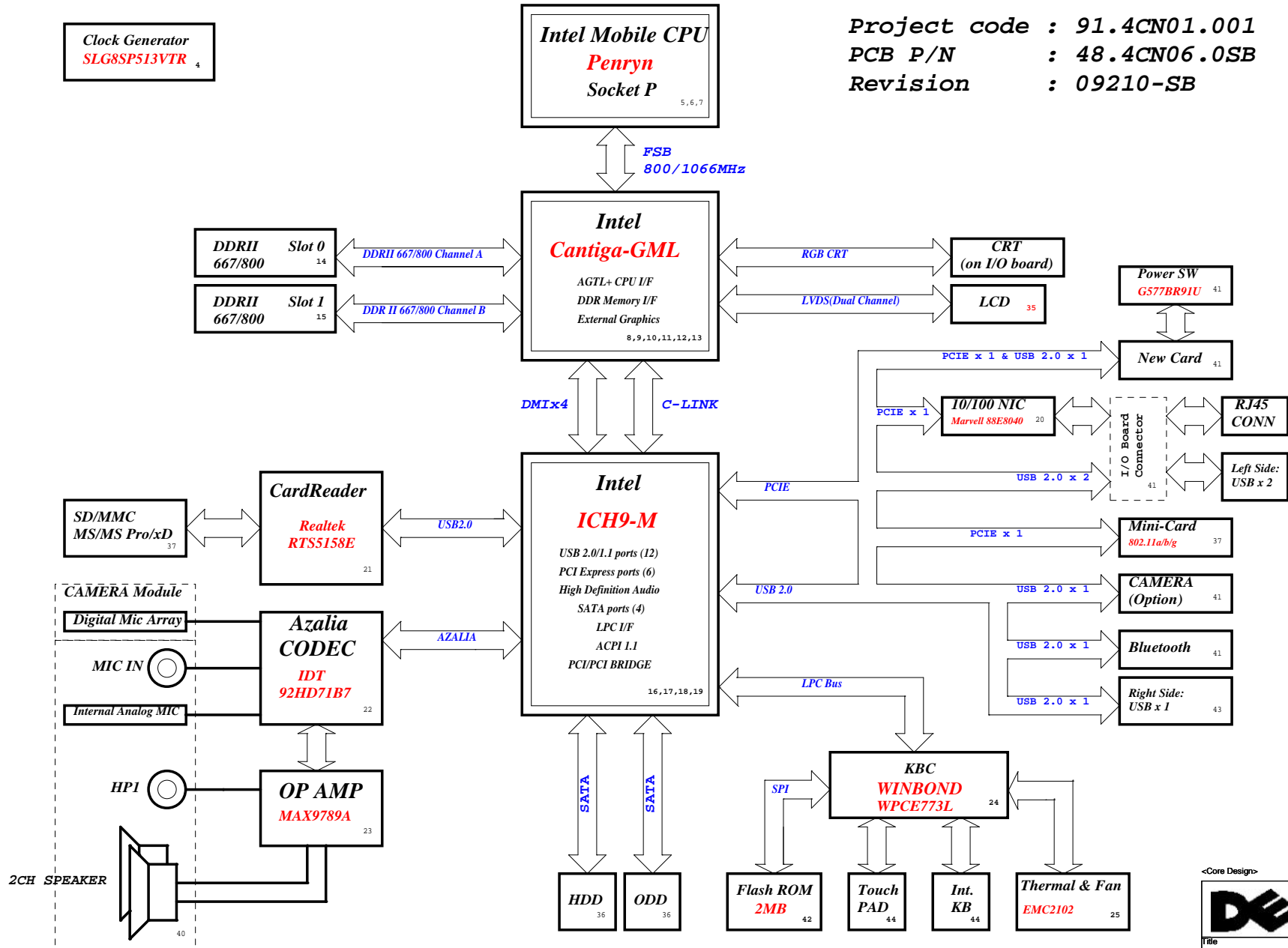
DR2 17" UMA

Rev
SB

Date: Monday, March 16, 2009

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Roberts Block Diagram



| | |
|---|---|
| CPU DC/DC ISL6266A 28, 29 | |
| INPUTS | OUTPUTS |
| +PWR_SRC | +VCC_CORE |
| SYSTEM DC/DC TPS51117 30 | |
| INPUTS | OUTPUTS |
| +PWR_SRC | +1.05V_VCCP |
| SYSTEM DC/DC MAX17020 27 | |
| INPUTS | OUTPUTS |
| +PWR_SRC | +5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW |
| SYSTEM DC/DC TPS51116 31 | |
| INPUTS | OUTPUTS |
| +PWR_SRC | +1.8V_SUS +0.9V_DDR_VTT +V_DDR_MCH_REF |
| SYSTEM DC/DC APL5912 32 | |
| INPUTS | OUTPUTS |
| +1.8V_SUS | +1.5V_RUN |
| SYSTEM DC/DC LDO 34 | |
| INPUTS | OUTPUTS |
| +5V_ALW | +5V_RUN |
| +3.3V_ALW | +3.3V_RUN |
| MAXIM CHARGER MAX8731A 26 | |
| INPUTS | OUTPUTS |
| +DC_IN | +PWR_SRC |
| +PBATT | |
| PCB LAYER | |
| L1: Top L2: VCC L3: Signal L4: Signal L5: GND L6: Bottom | |

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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

| Signal | Usage/When Sampled | Comment |
|-------------------------------|--|---|
| HDA_SDOUT | XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK. | Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down. |
| HDA_SYNC | PCIE config1 bit0, Rising Edge of PWROK. | This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h). |
| GNT2#/ GPIO53 | PCIE config2 bit2, Rising Edge of PWROK. | This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h). |
| GPIO20 | Reserved. | This signal should not be pulled high. |
| GNT1#/ GPIO51 | ESI Strap (Server Only) Rising Edge of PWROK. | ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile. |
| GNT3#/ GPIO55 | Top-Block Swap override. Rising Edge of PWROK. | Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space) Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down. |
| GNT0#: SPI_CS1#/ GPIO58 | Boot BIOS Destination Selection 0:1. Rising Edge of PWROK. | Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC |
| SPI_MOSI | Integrated TPM Enable, Rising Edge of CLPWROK. | Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable. |
| GPIO49 | DMI Termination Voltage. Rising Edge of CLPWROK. | The signal is required to be low for desktop applications and required to be high for mobile applications. |
| SATALED# | PCI Express Lane Reversal. Rising Edge of PWROK. | Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8). |
| SPKR | No Reboot. Rising Edge of PWROK. | If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit. |
| TP3 | XOR Chain Entrance. Rising Edge of PWROK. | This signal should not be pull low unless using XOR Chain testing. |
| GPIO33/ HDA_DOCK _EN# | Flash Descriptor Security Override Strap. Rising Edge of PWROK. | Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor. |

ICH9 Integrated pull-up
and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

| SIGNAL | Resistor Type/Value |
|--------------------------|---|
| CL_CLK[1:0] | PULL-UP 20K |
| CL_DATA[1:0] | PULL-UP 20K |
| CL_RST0# | PULL-UP 20K |
| DPRSLPVR/GPIO16 | PULL-DOWN 20K |
| ENERGY_DETECT | PULL-UP 20K |
| HDA_BIT_CLK | PULL-DOWN 20K |
| HDA_DOCK_EN#/GPIO33 | PULL-UP 20K |
| HDA_RST# | PULL-DOWN 20K |
| HDA_SDIN[3:0] | PULL-DOWN 20K |
| HDA_SDOUT | PULL-DOWN 20K |
| HDA_SYNC | PULL-DOWN 20K |
| GLAN_DOCK# | The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller. |
| GNT[3:0]#/GPIO[55,53,51] | PULL-UP 20K |
| GPIO20 | PULL-DOWN 20K |
| GPIO49 | PULL-UP 20K |
| LDA[3:0]#/FWH[3:0]# | PULL-UP 20K |
| LAN_RXD[2:0] | PULL-UP 20K |
| LDRQ[0] | PULL-UP 20K |
| LDRQ[1]/GPIO23 | PULL-UP 20K |
| PME# | PULL-UP 20K |
| PWRBTN# | PULL-UP 20K |
| SATALED# | PULL-UP 15K |
| SPI_CS1#/GPIO58/CLGPIO6 | PULL-UP 20K |
| SPI_MOSI | PULL-DOWN 20K |
| SPI_MISO | PULL-UP 20K |
| SPKR | PULL-DOWN 20K |
| TACH_[3:0] | PULL-UP 20K |
| TP[3] | PULL-UP 20K |
| USB[11:0][P,N] | PULL-DOWN 15K |

Cantiga chipset and ICH9M I/O controller
Hub strapping configuration

Montevina Platform Design guide 22339 Rev.0.5

| Pin Name | Strap Description | Configuration |
|--|---|---|
| CFG[2:0] | FSB Frequency Select | 000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved |
| CFG[4:3] CFG8 CFG[15:14] CFG[18:17] | Reserved | |
| CFG5 | DMI x2 Select | 0 = DMI x2 1 = DMI x4 (Default) |
| CFG6 | iTPM Host Interface | 0 = The iTPM Host Interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default) |
| CFG7 | Intel Management engine crypto strap | 0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality(Default) |
| CFG9 | PCIE Graphics Lane | 0 = Reserved Lanes, 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in Order |
| CFG10 | PCIE Loopback enable | 0 = Enable (Note 3) 1 = Disable (Default) |
| CFG[13:12] | XOR/ALL | 00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) 11 = Disabled (Default) |
| CFG16 | FSB Dynamic ODT | 0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default) |
| CFG19 | DMI Lane Reversal | 0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1) |
| CFG20 | Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE | 0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simultaneously via the PEG port |
| SDVO _CTRLDATA | SDVO Present | 0 = No SDVO Card Present (Default) 1 = SDVO Card Present |
| L_DDC_DATA | Local Flat Panel (LFP) Present | 0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled |

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

PCIE Routing

| | |
|-------|---------------|
| | |
| LANE2 | MiniCard WLAN |
| LANE3 | LAN |
| LANE5 | New Card |

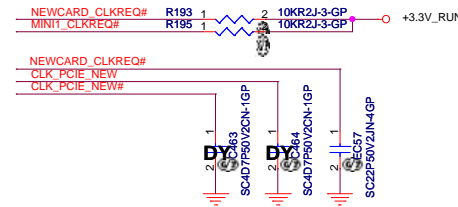
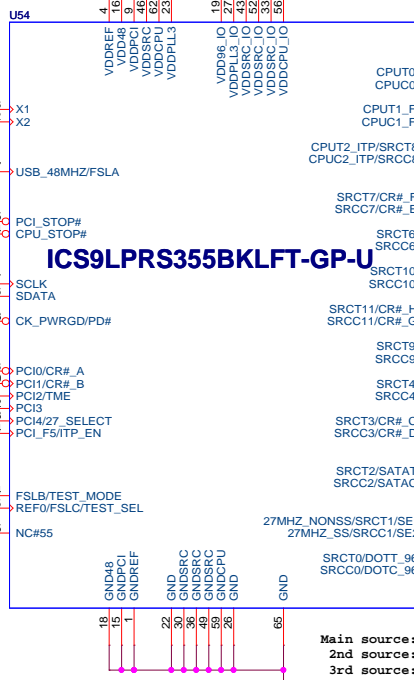
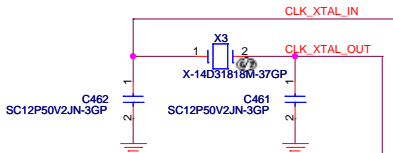
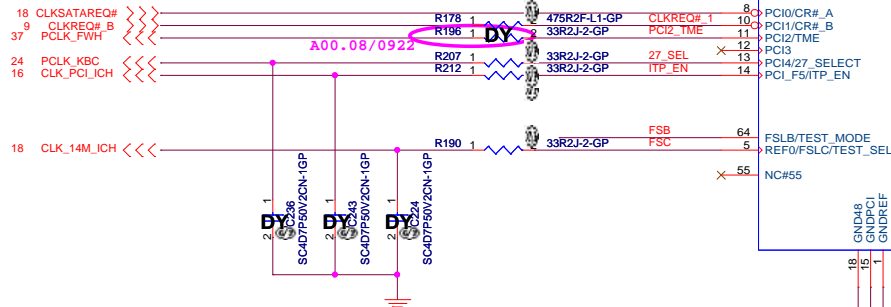
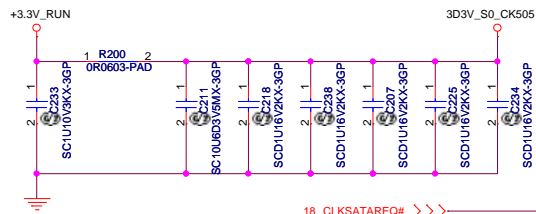
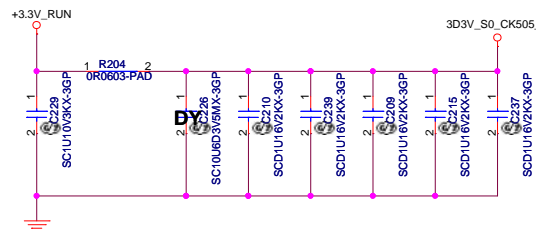
USB Table

| USB | |
|------|-------------|
| Pair | Device |
| 0 | USB1 |
| 1 | USB2 |
| 2 | USB3 |
| 3 | RESERVED |
| 4 | MINI CARD |
| 5 | RESERVED |
| 6 | BLUETOOTH |
| 7 | NEW CARD |
| 8 | RESERVED |
| 9 | RESERVED |
| 10 | Card Reader |
| 11 | CAMERA |

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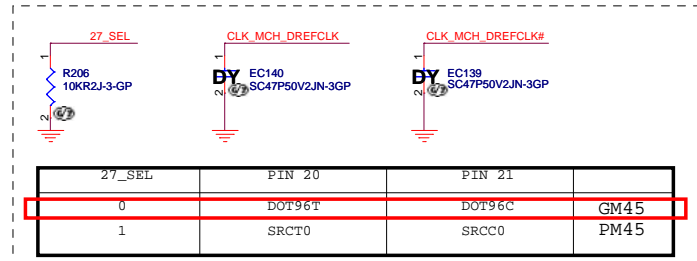
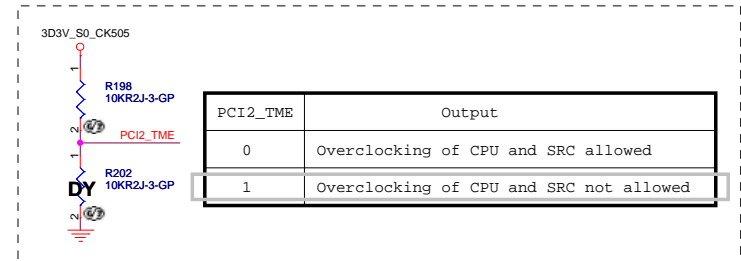
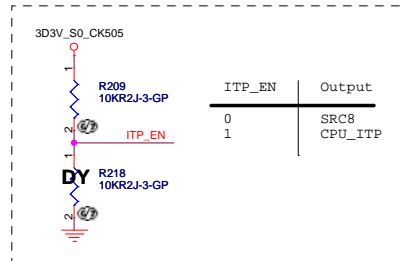
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| Title | | | |
| Table of Content | | | |
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SSID = CLOCK

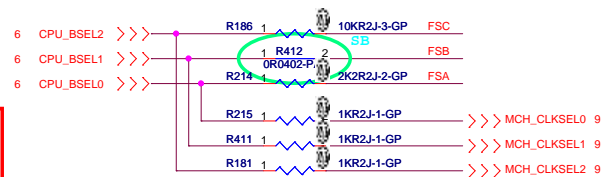


Main source: 71.08513.003 (SLG8SP513VTR)
2nd source: 71.00875.C03 (RTM875N-606-VD-GRT)
3rd source:

Co-layout Ref: 71.09355.B03 (ICS9LPRS355BKLFT)



| SEL2 FSC | SEL1 FSB | SEL0 FSA | CPU | FSB |
|-------------|-------------|-------------|------|-------|
| 1 | 0 | 1 | 100M | X |
| 0 | 0 | 1 | 133M | 533M |
| 0 | 1 | 1 | 166M | 667M |
| 0 | 1 | 0 | 200M | 800M |
| 0 | 0 | 0 | 266M | 1067M |



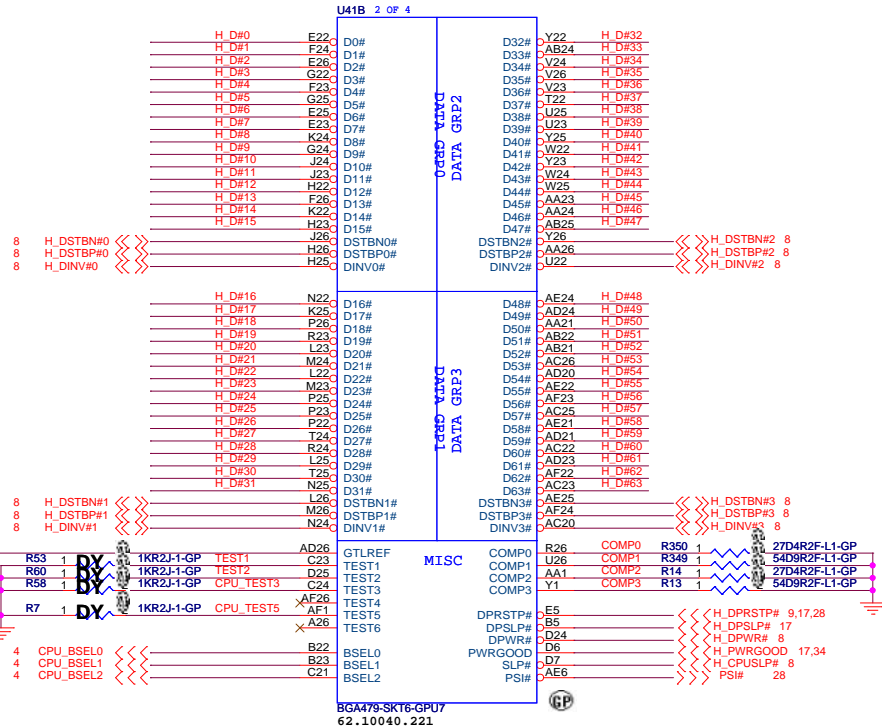
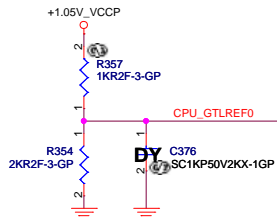
SSID = CPU



H_THRMTRIP# should connect to ICH9 and MCH without T-ing.

H_DINV#[3..0] <<>> H_DINV#[3..0] 8
 H_DSTBN#[3..0] <<>> H_DSTBN#[3..0] 8
 H_DSTBP#[3..0] <<>> H_DSTBP#[3..0] 8
 H_D# [63..0] <<>> H_D# [63..0] 8

Layout notes
 Z= 55 Ohm 0.5" MAX for CPU_GTLREF0

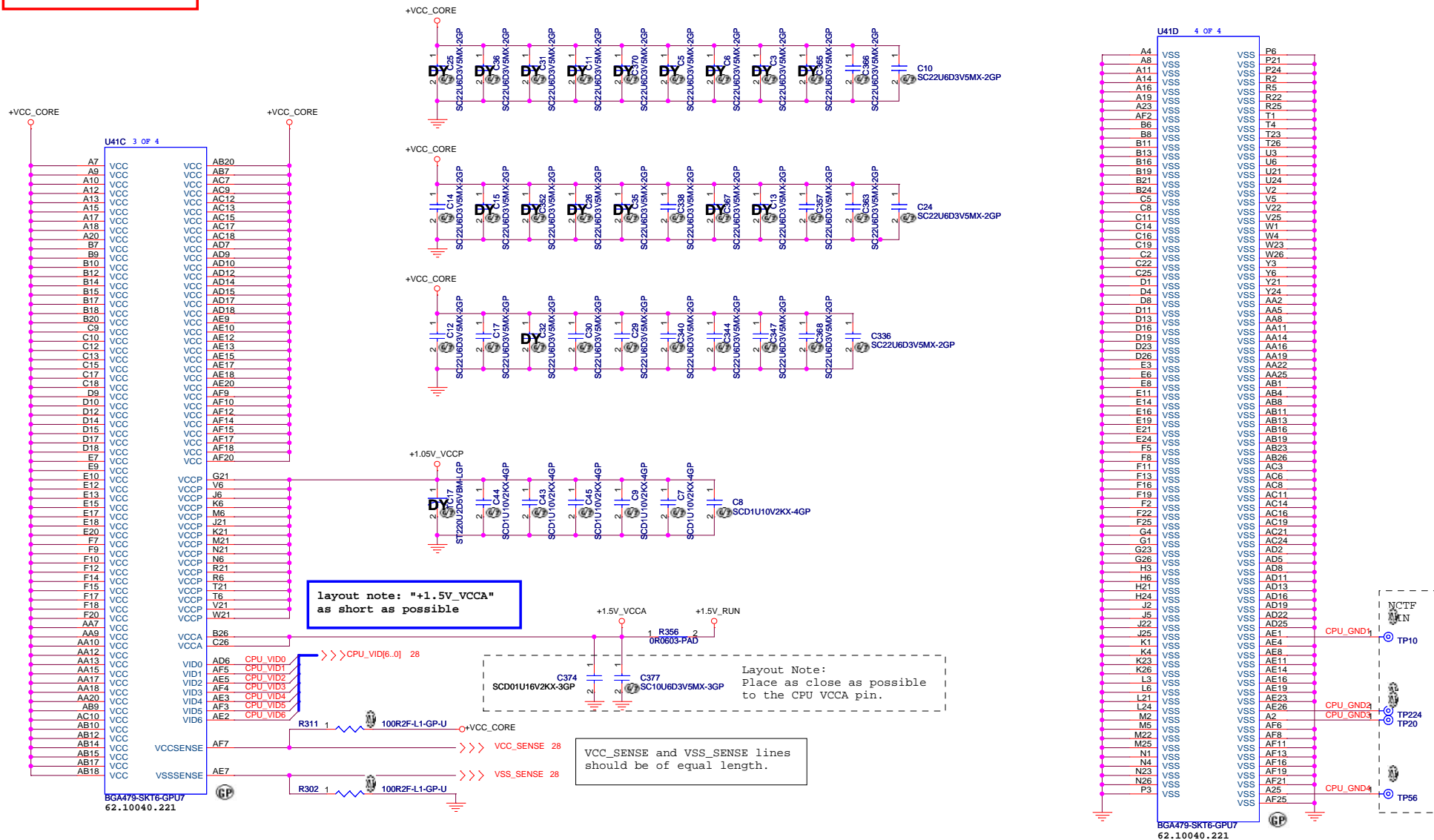


Layout Note:
 Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
 Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

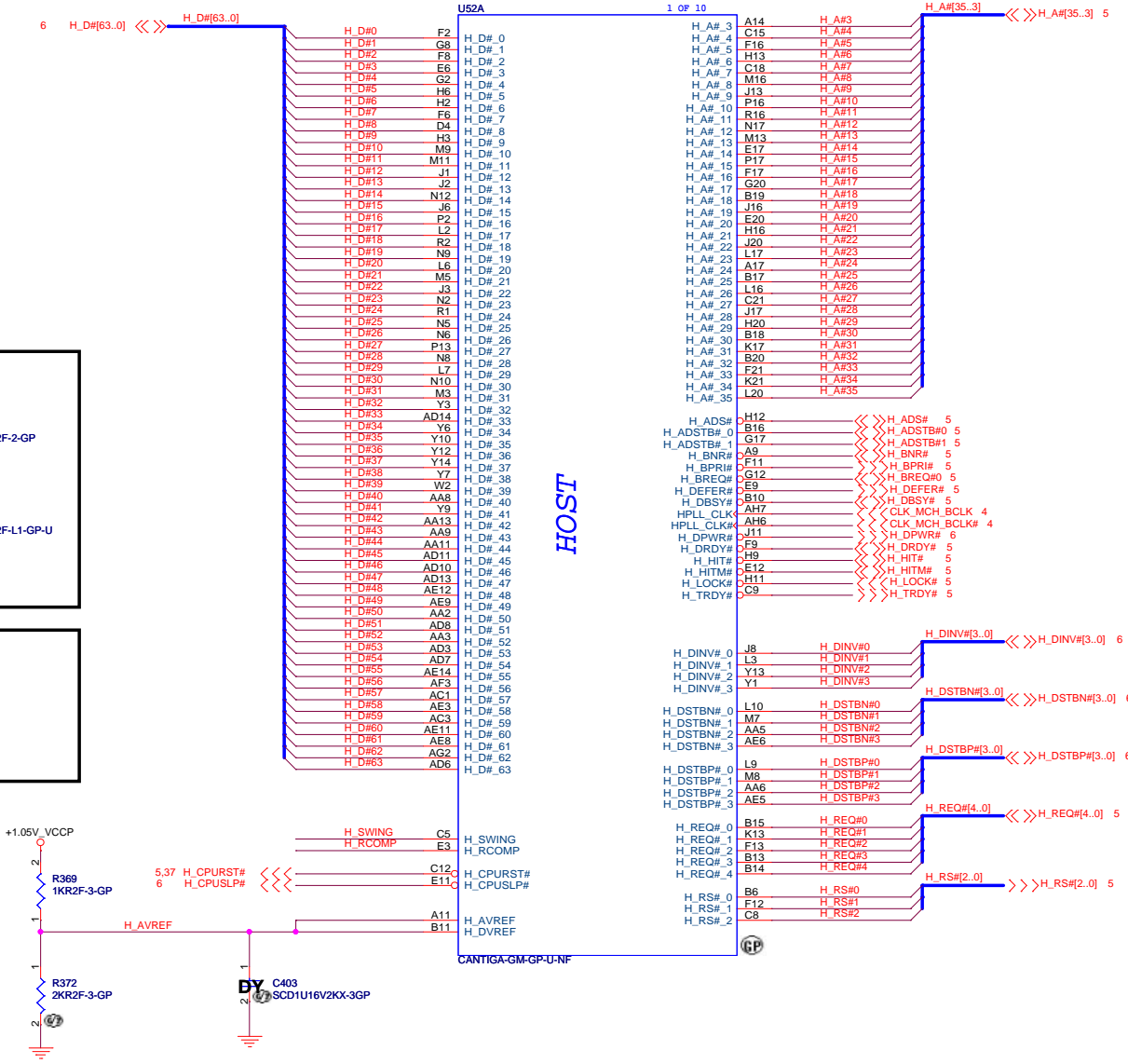
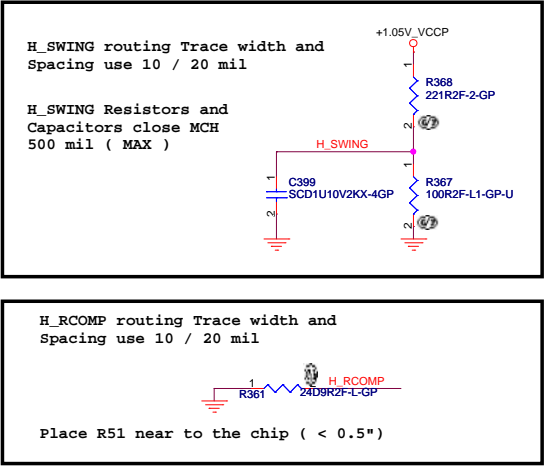
Route the CPU_TEST3 and CPU_TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

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SSID = CPU



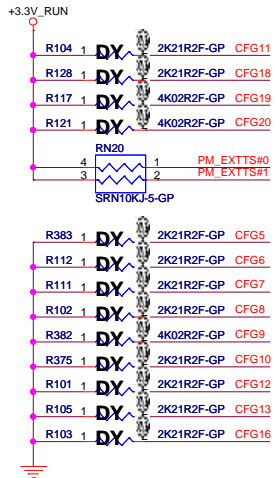
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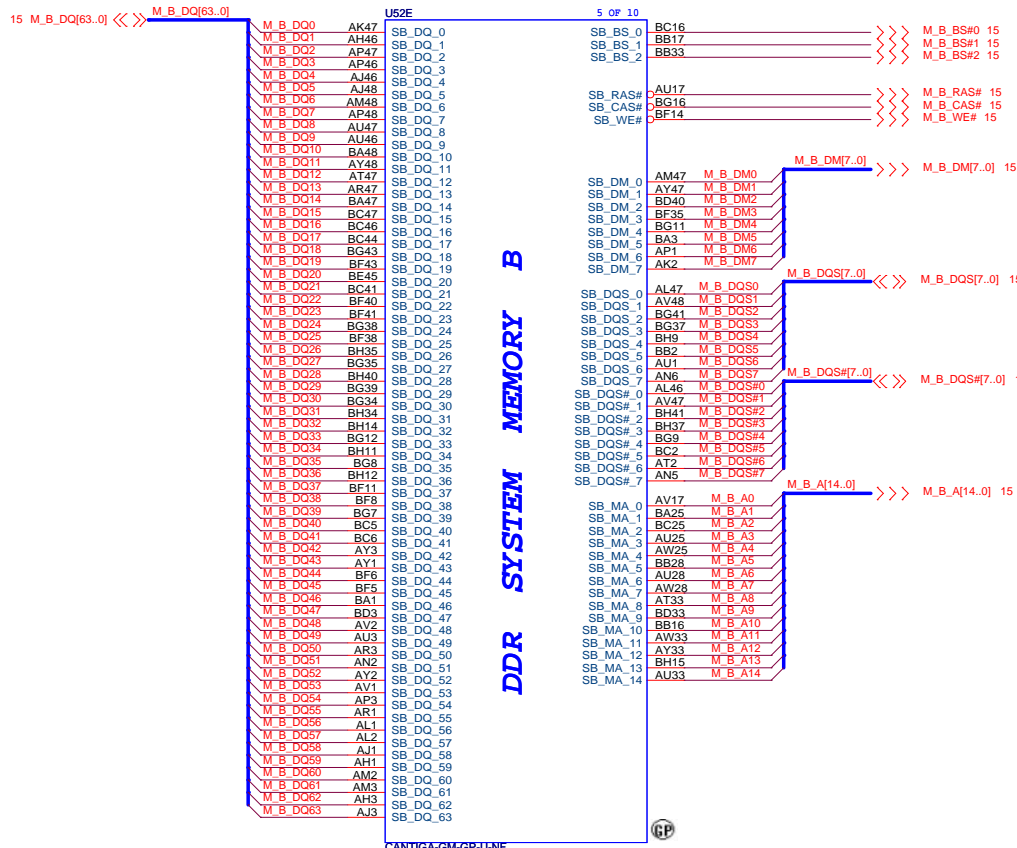
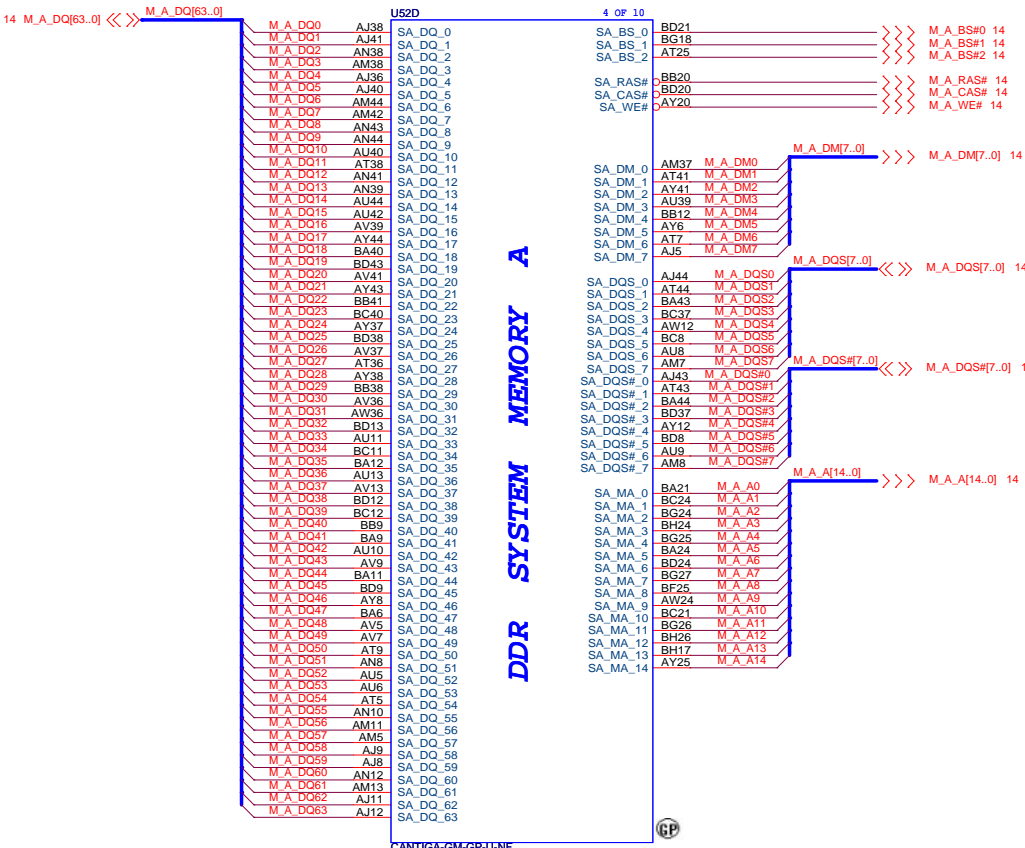
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* is current setting

| CFG Strap | Low | High |
|---------------|--|---|
| CFG 5 | DMI X 2 | DMI X 4 * |
| CFG 6 | ITPM enable | ITPM disable * |
| CFG 7 | TLS cipher suite with no confidentiality | TLS cipher suite with confidentiality * |
| CFG 9 | PCIE GFX lane reversed | PCIE GFX lane numbered in order * |
| CFG 10 | PCIE loopback enable | PCIE loopback disable * |
| CFG 12 | ALLZ mode enable | ALLZ mode disable * |
| CFG 13 | XOR mode enable | XOR mode disable * |
| CFG 16 | FSB dynamic ODT disable | FSB Dynamic ODT enable * |
| CFG 19 | Normal operation * | Reverse DMI lanes |
| CFG 20 | SDVO concurrent with PCIE * | PCIE and SDVO are operating simultaneously via the PEG port * |
| SDVO_CTRLDATA | SDVO interface disable * | SDVO interface enable |
| L_DDC_DATA | LFP disable * | LFP card present |
| DDPC_CTRLDATA | SDVO/iHDMI/DP interface disabled * | SDVO/iHDMI/DP interface enabled |



SSID = MCH



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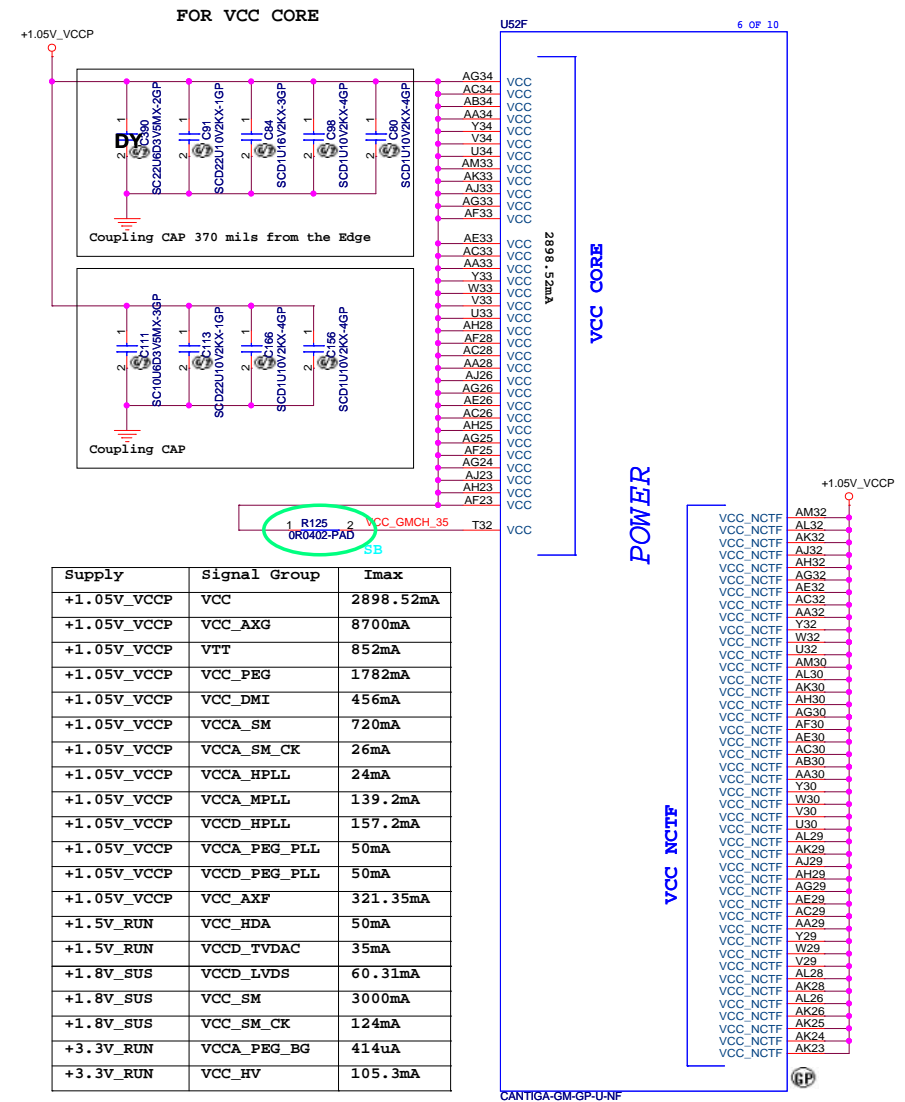
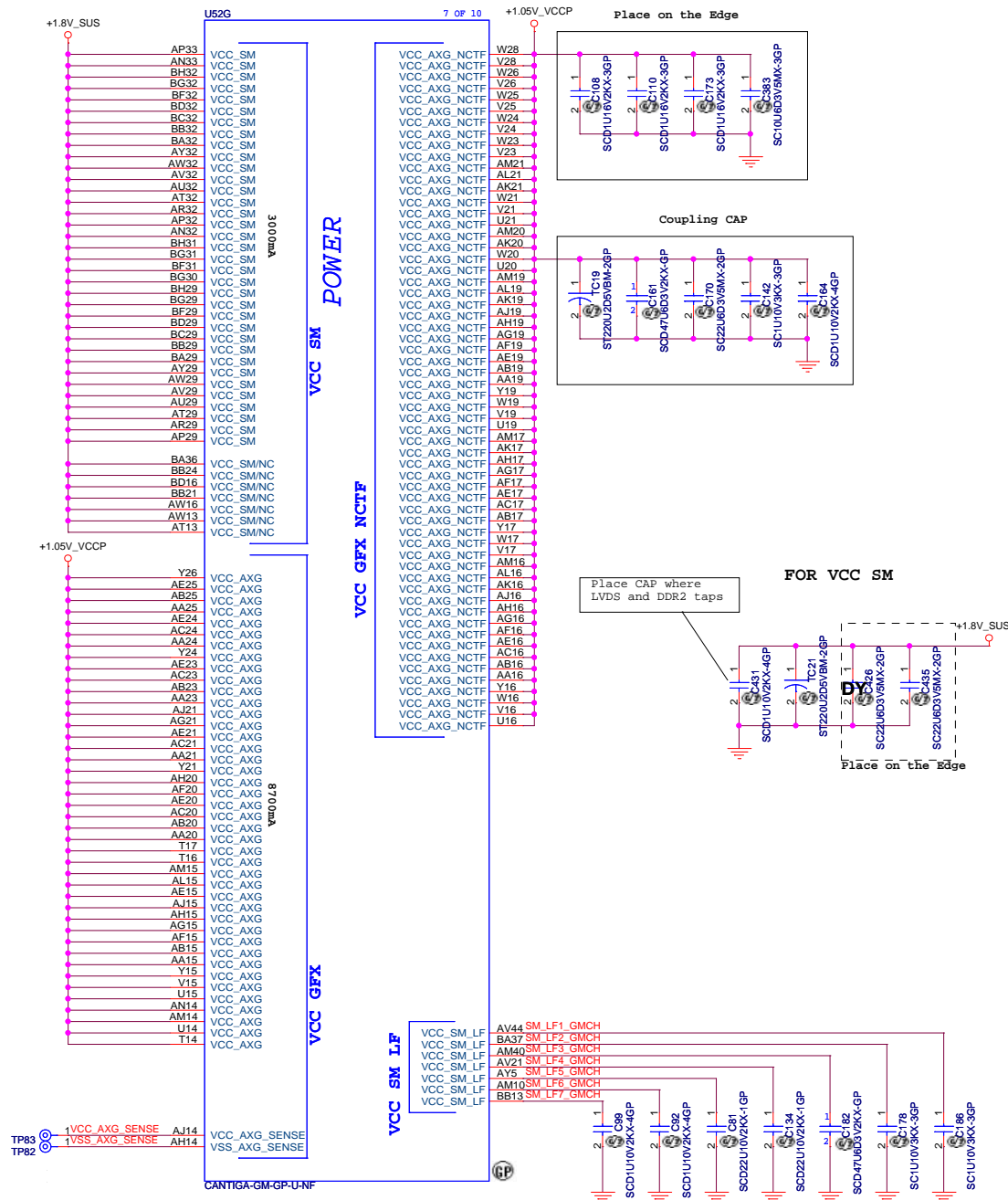
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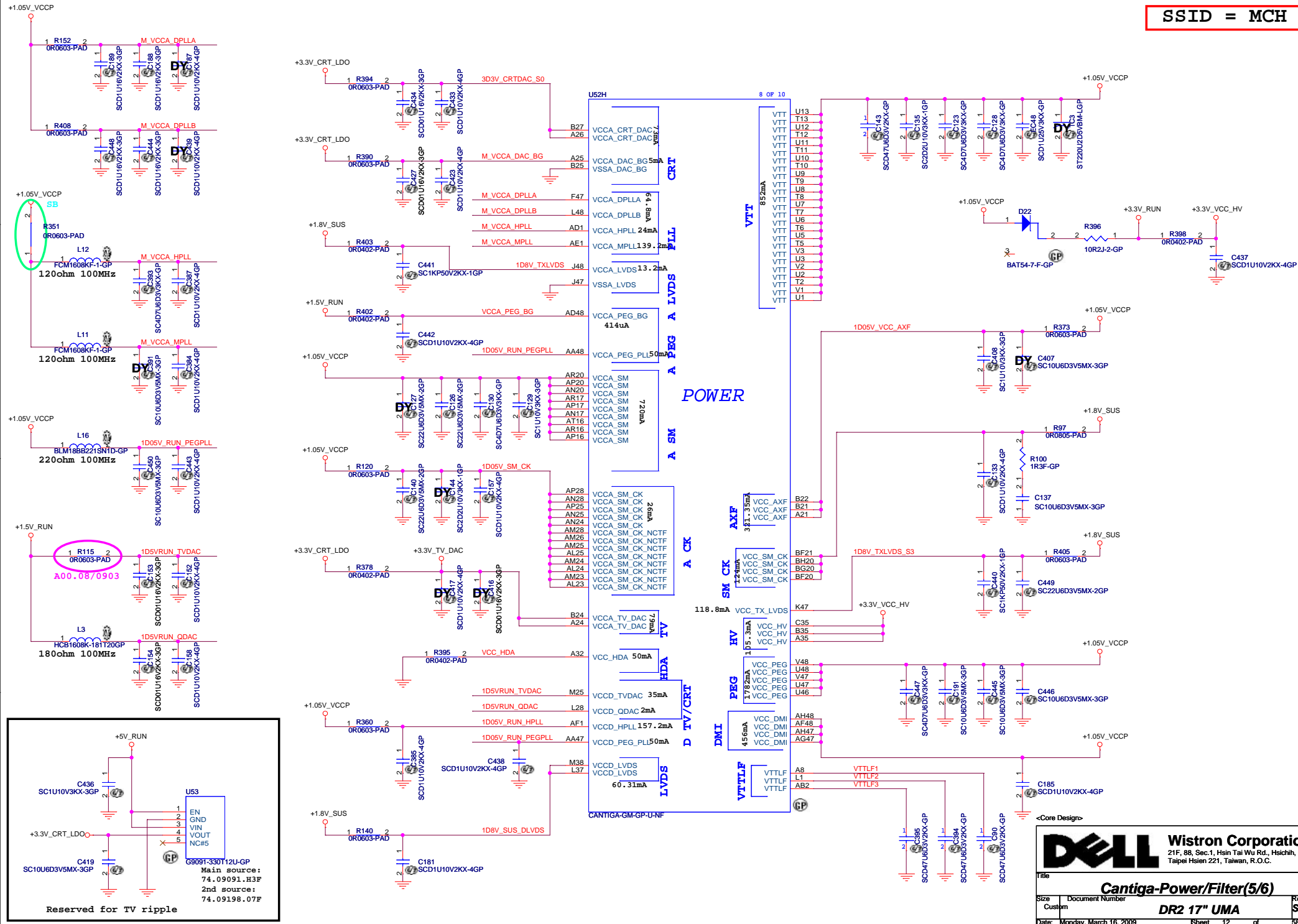
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| Custom | DR2 17" UMA | S |
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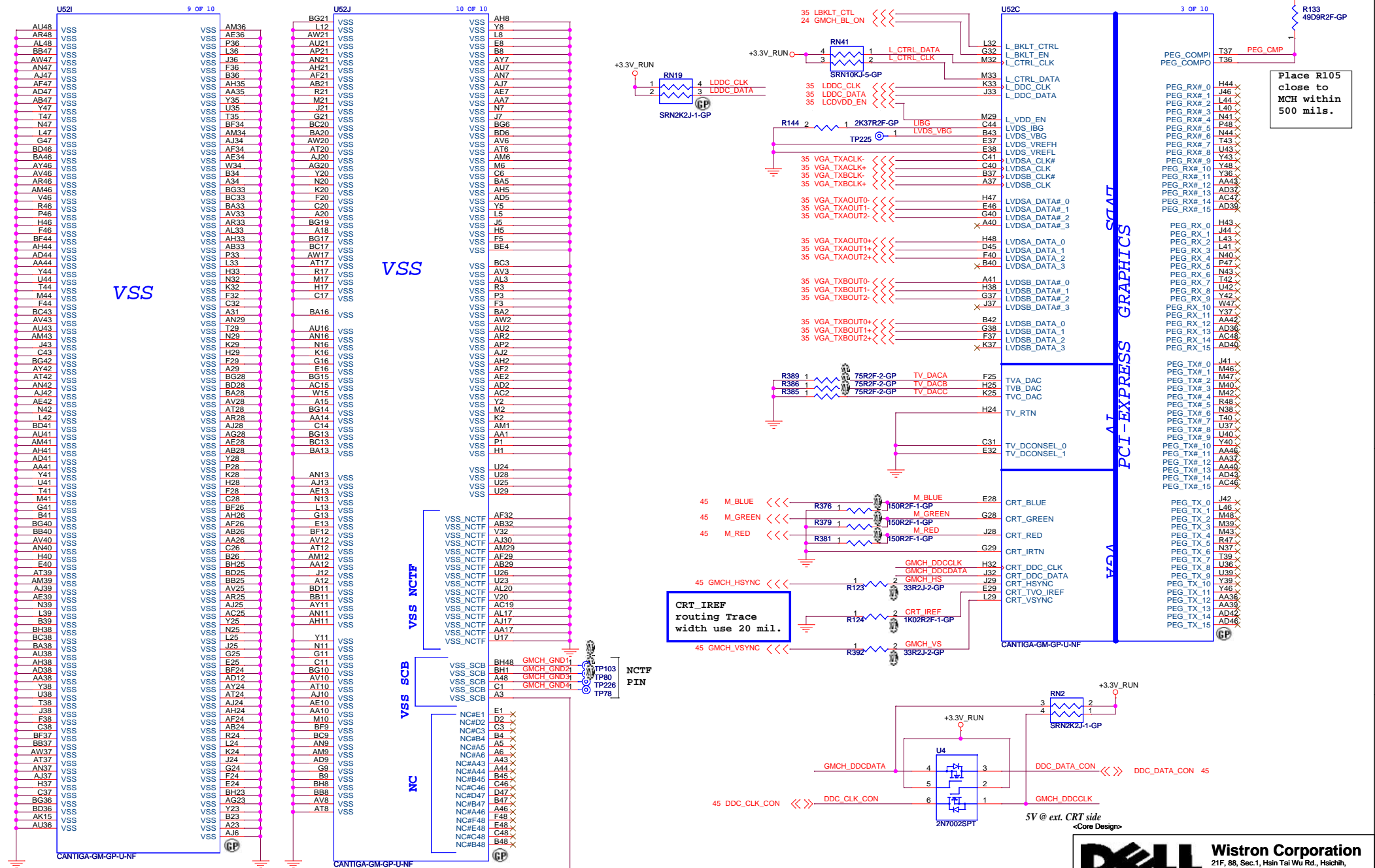
SSID = MCH



| Supply | Signal Group | I _{max} |
|-------------|--------------|------------------|
| +1.05V_VCCP | VCC | 2898.52mA |
| +1.05V_VCCP | VCC_AXG | 8700mA |
| +1.05V_VCCP | VIT | 852mA |
| +1.05V_VCCP | VCC_PEG | 1782mA |
| +1.05V_VCCP | VCC_DMI | 456mA |
| +1.05V_VCCP | VCCA_SM | 720mA |
| +1.05V_VCCP | VCCA_SM_CK | 26mA |
| +1.05V_VCCP | VCCA_HPLL | 24mA |
| +1.05V_VCCP | VCCA_MPLL | 139.2mA |
| +1.05V_VCCP | VCCD_HPLL | 157.2mA |
| +1.05V_VCCP | VCCA_PEG_PLL | 50mA |
| +1.05V_VCCP | VCCD_PEG_PLL | 50mA |
| +1.05V_VCCP | VCC_AXF | 321.35mA |
| +1.5V_RUN | VCC_HDA | 50mA |
| +1.5V_RUN | VCCD_TVDDAC | 35mA |
| +1.8V_SUS | VCCD_LVDS | 60.31mA |
| +1.8V_SUS | VCC_SM | 3000mA |
| +1.8V_SUS | VCC_SM_CK | 124mA |
| +3.3V_RUN | VCCA_PEG_BG | 414uA |
| +3.3V_RUN | VCC_HV | 105.3mA |



SSID = MCH



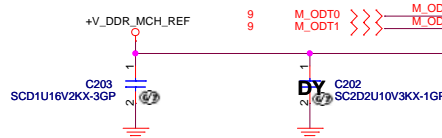
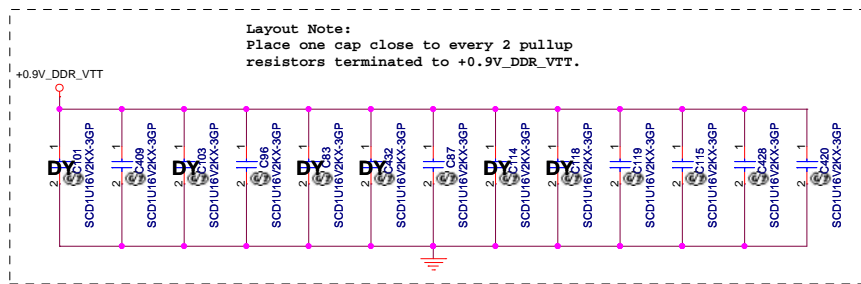
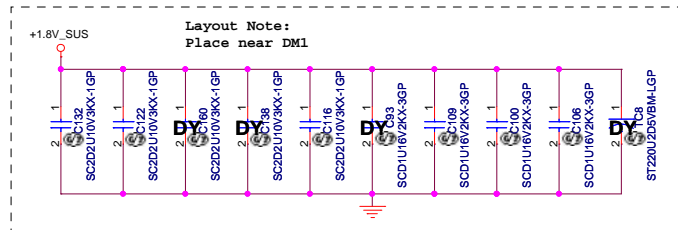
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10 M_A_DQ[63..0] << >> _____

10 M_A_DM[7..0] << >> _____

10 M_A_DQS[7..0] << >> _____

10 M_A_A[14..0] << >> _____

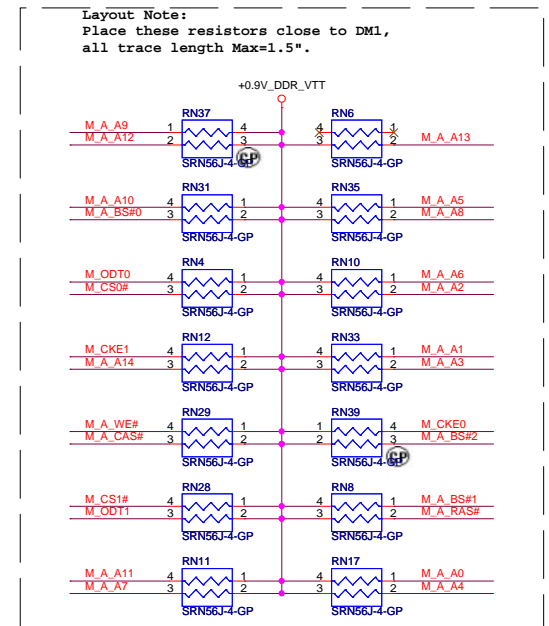
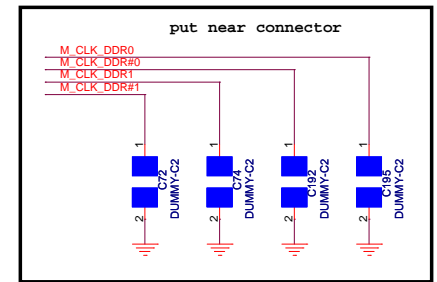


| | | |
|----------|-----|----------------|
| M_A A0 | 102 | A0 |
| M_A A1 | 101 | A1 |
| M_A A2 | 100 | A2 |
| M_A A3 | 99 | A3 |
| M_A A4 | 98 | A4 |
| M_A A5 | 97 | A5 |
| M_A A6 | 94 | A6 |
| M_A A7 | 92 | A7 |
| M_A A8 | 93 | A8 |
| M_A A9 | 91 | A9 |
| M_A A10 | 105 | A10/AP |
| M_A A11 | 90 | A11 |
| M_A A12 | 89 | A12 |
| M_A A13 | 116 | A13 |
| M_A A14 | 86 | A14 |
| M_A BS#2 | 85 | A15 #16/BA2 |
| M_A BS#0 | 107 | BA0 |
| M_A BS#1 | 106 | BA1 |

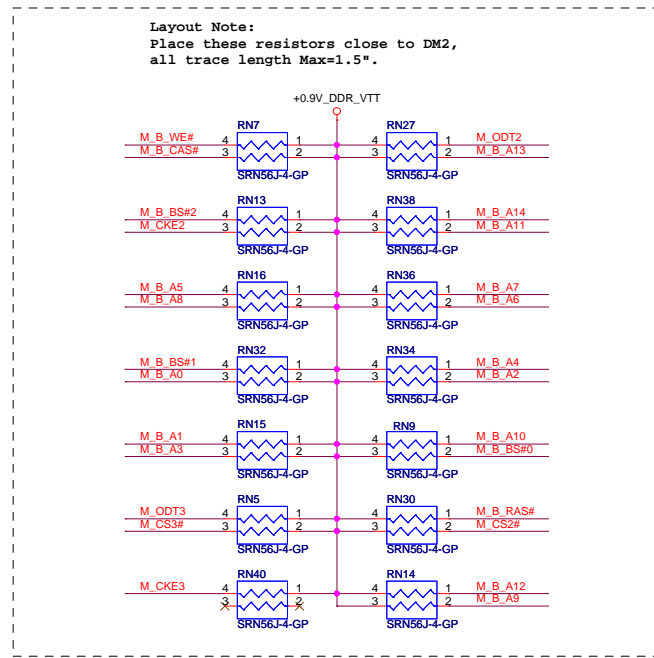
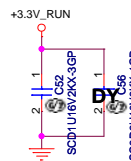
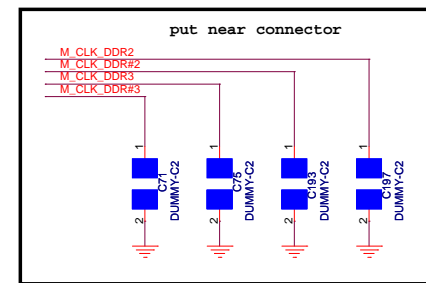
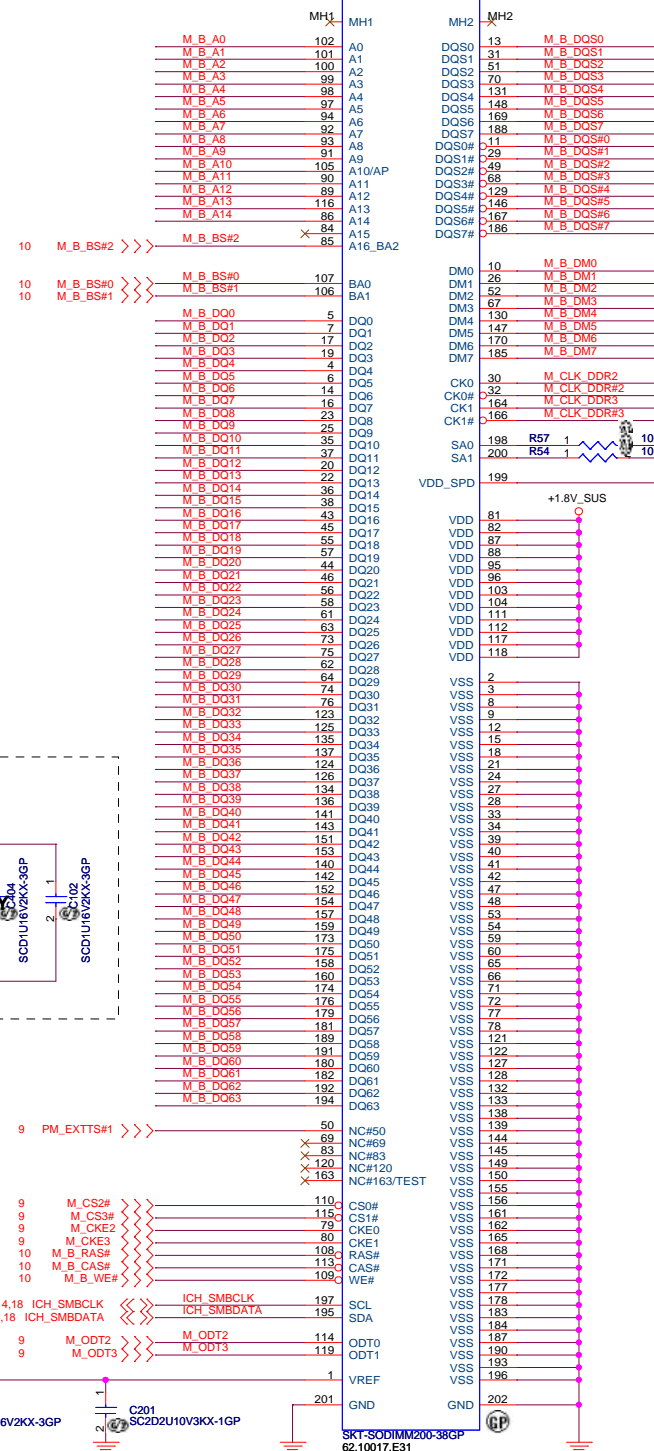
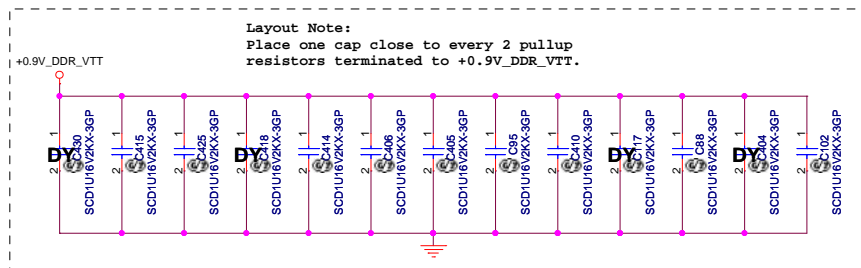
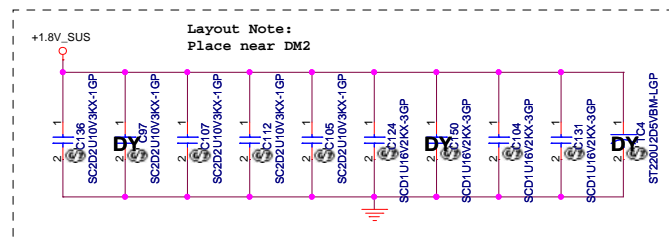
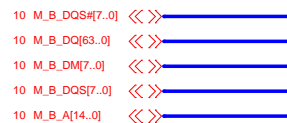
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| M.A.D01 | 7 | D01 |
| M.A.D02 | 17 | D02 |
| M.A.D03 | 9 | D03 |
| M.A.D04 | 4 | D04 |
| M.A.D05 | 6 | D05 |
| M.A.D06 | 14 | D06 |
| M.A.D07 | 16 | D07 |
| M.A.D08 | 23 | D08 |
| M.A.D09 | 25 | D09 |
| M.A.D010 | 35 | D010 |
| M.A.D011 | 37 | D011 |
| M.A.D012 | 22 | D012 |
| M.A.D013 | 22 | D013 |
| M.A.D014 | 36 | D014 |
| M.A.D015 | 38 | D015 |
| M.A.D016 | 43 | D016 |
| M.A.D017 | 45 | D017 |
| M.A.D018 | 55 | D018 |
| M.A.D019 | 57 | D019 |
| M.A.D020 | 40 | D020 |
| M.A.D021 | 44 | D021 |
| M.A.D022 | 56 | D022 |
| M.A.D023 | 58 | D023 |
| M.A.D024 | 61 | D024 |
| M.A.D025 | 63 | D025 |
| M.A.D026 | 73 | D026 |
| M.A.D027 | 75 | D027 |
| M.A.D028 | 68 | D028 |
| M.A.D029 | 64 | D029 |
| M.A.D030 | 74 | D030 |
| M.A.D031 | 76 | D031 |
| M.A.D032 | 123 | D032 |
| M.A.D033 | 125 | D033 |
| M.A.D034 | 137 | D034 |
| M.A.D035 | 137 | D035 |
| M.A.D036 | 124 | D036 |
| M.A.D037 | 126 | D037 |
| M.A.D038 | 136 | D038 |
| M.A.D039 | 136 | D039 |
| M.A.D040 | 141 | D040 |
| M.A.D041 | 143 | D041 |
| M.A.D042 | 151 | D042 |
| M.A.D043 | 152 | D043 |
| M.A.D044 | 140 | D044 |
| M.A.D045 | 142 | D045 |
| M.A.D046 | 152 | D046 |
| M.A.D047 | 154 | D047 |
| M.A.D048 | 157 | D048 |
| M.A.D049 | 159 | D049 |
| M.A.D050 | 173 | D050 |
| M.A.D051 | 175 | D051 |
| M.A.D052 | 158 | D052 |
| M.A.D053 | 160 | D053 |
| M.A.D054 | 174 | D054 |
| M.A.D055 | 176 | D055 |
| M.A.D056 | 176 | D056 |
| M.A.D057 | 181 | D057 |
| M.A.D058 | 189 | D058 |
| M.A.D059 | 191 | D059 |
| M.A.D060 | 189 | D060 |
| M.A.D061 | 182 | D061 |
| M.A.D062 | 192 | D062 |
| M.A.D063 | 194 | D063 |

| | | |
|-----------|-----|-------|
| M.A.DOS#0 | 11 | DOS#0 |
| M.A.DOS#1 | 29 | DOS#1 |
| M.A.DOS#2 | 29 | DOS#2 |
| M.A.DOS#3 | 68 | DOS#3 |
| M.A.DOS#4 | 129 | DOS#4 |
| M.A.DOS#5 | 146 | DOS#5 |
| M.A.DOS#6 | 167 | DOS#6 |
| M.A.DOS#7 | 186 | DOS#7 |
| | | |
| M.A.DOS0 | 13 | DOS0 |
| M.A.DOS1 | 31 | DOS1 |
| M.A.DOS2 | 51 | DOS2 |
| M.A.DOS3 | 70 | DOS3 |
| M.A.DOS4 | 131 | DOS4 |
| M.A.DOS5 | 148 | DOS5 |
| M.A.DOS6 | 169 | DOS6 |
| M.A.DOS7 | 188 | DOS7 |

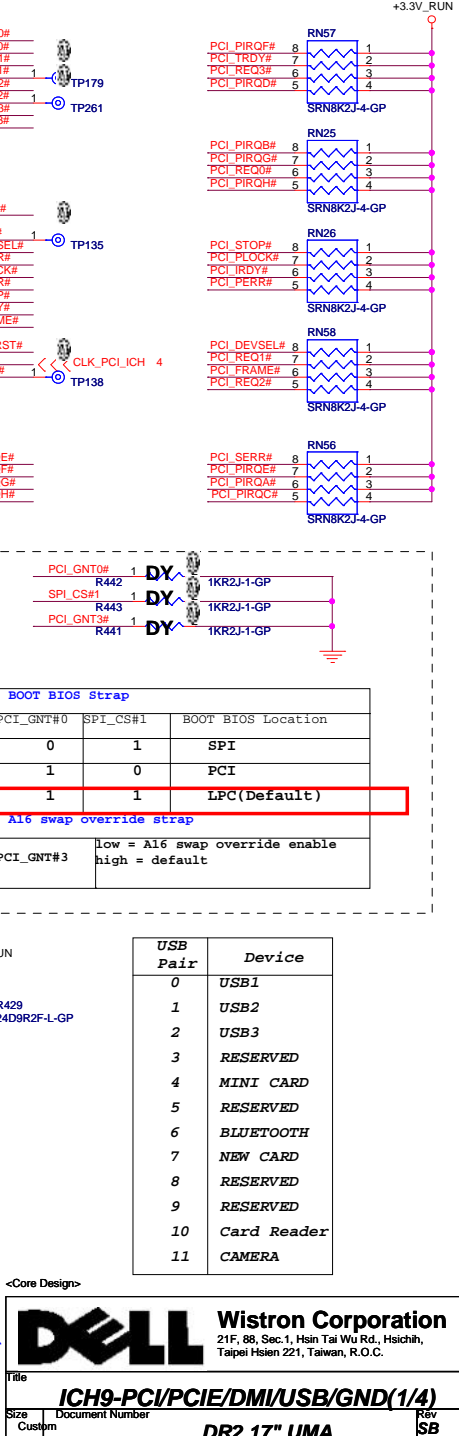
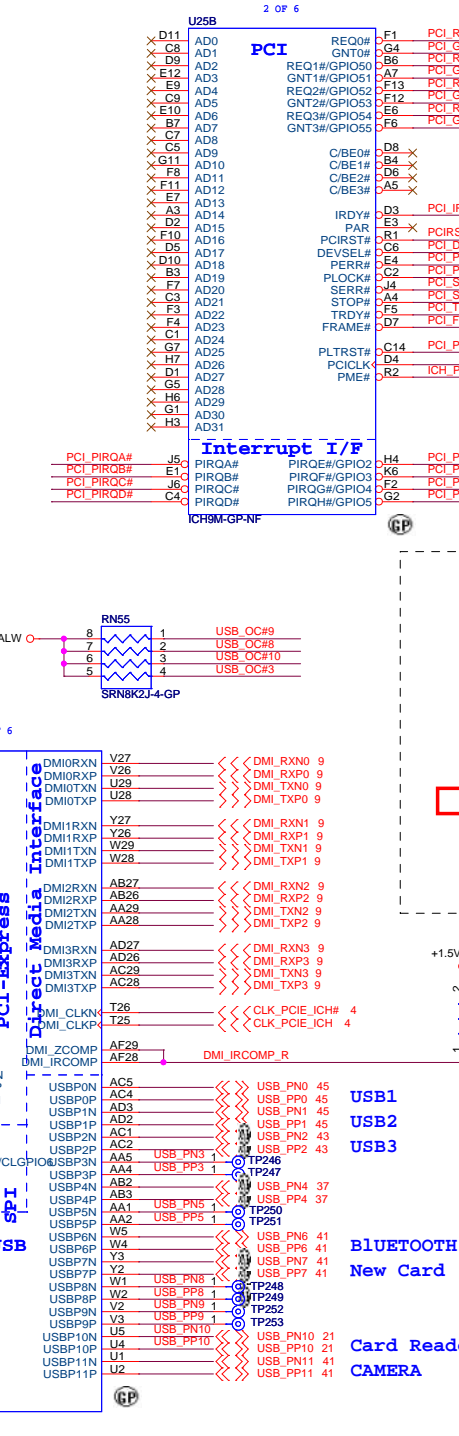
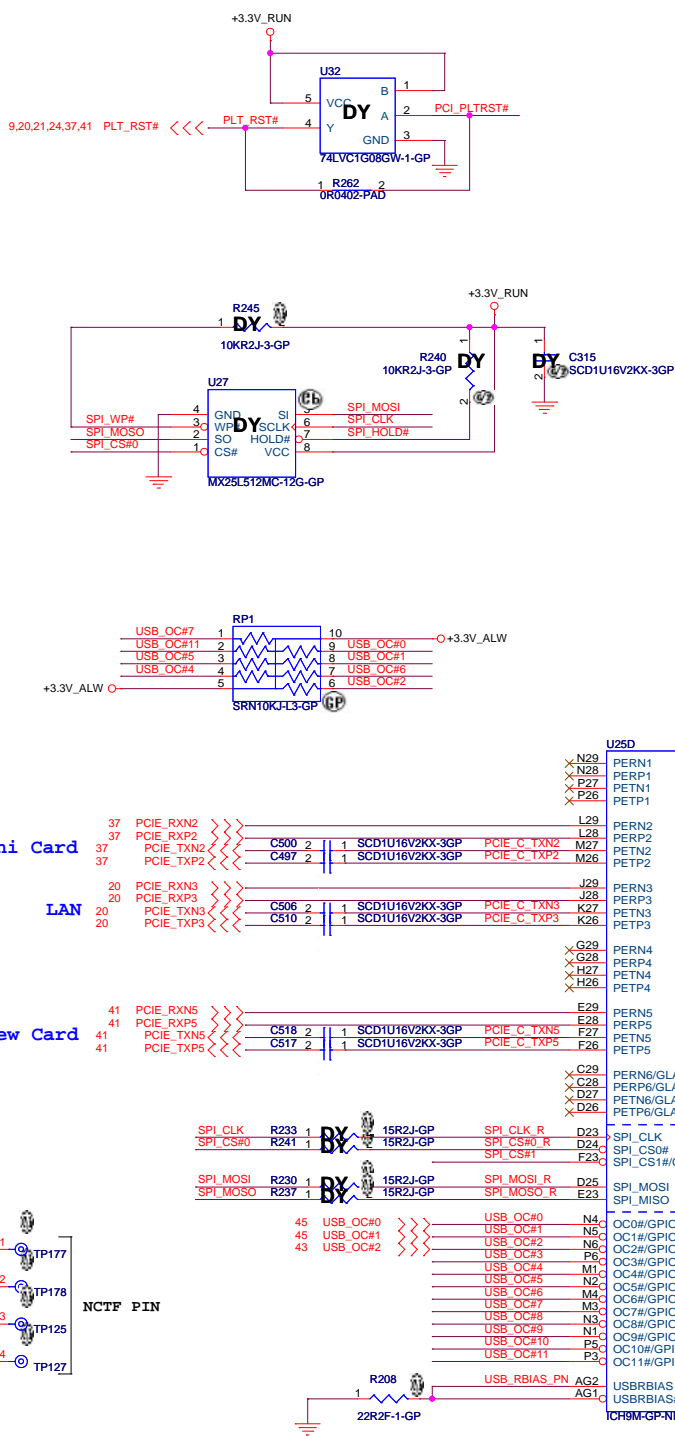
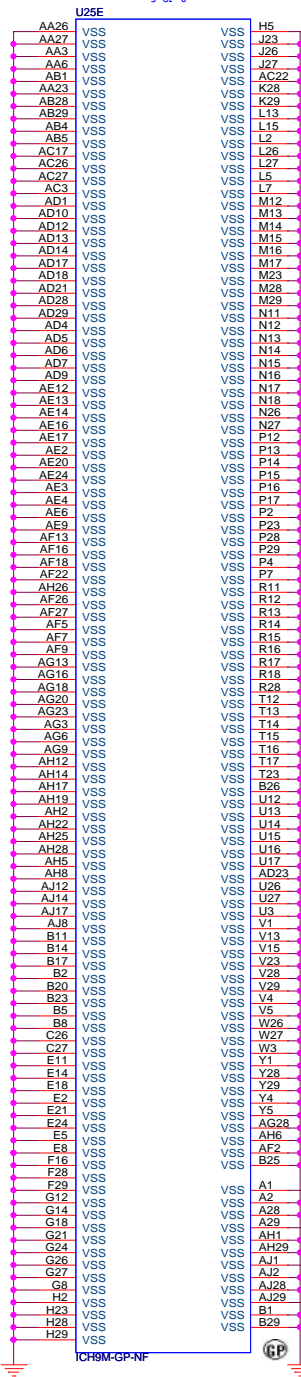
The image displays the bottom layer of a PCB layout. It includes various component footprints such as resistors (R55, R56), capacitors (C10, C11), and integrated circuits (U1, U2). A detailed pin list is provided on the right side, mapping pin numbers to component names and functions. The list includes pins for RAS#, WE#, CAS#, CS0#, CS1#, CKE0, CKE1, CK0, CK0#, CK1, CK1#, DM0, DM1, DM2, DM3, DM4, DM5, DM6, DM7, SDA, SCL, VDDSPD, SA0, SA1, NC#50, NC#69, NC#83, NC#120, NC#163/TEST, VDD, VSS, and GND. The layout also shows a 10KR2J-3-GP resistor and a 10KR2J-3-GP capacitor. The bottom right corner features a small schematic diagram of a component with pins labeled 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100.



SSID = MEMORY



SSID = ICH



| PCI_GNT#0 | SPI_CS#1 | BOOT BIOS Location |
|-----------|----------|--------------------|
| 0 | 1 | SPI |
| 1 | 0 | PCI |
| 1 | 1 | LPC(Default) |

Al6 swap override strap

| | |
|-----------|--|
| PCI_GNT#3 | low = Al6 swap override enable high = default |
|-----------|--|

| USB Pair | Device |
|----------|-------------|
| 0 | USB1 |
| 1 | USB2 |
| 2 | USB3 |
| 3 | RESERVED |
| 4 | MINI CARD |
| 5 | RESERVED |
| 6 | BLUETOOTH |
| 7 | NEW CARD |
| 8 | RESERVED |
| 9 | RESERVED |
| 10 | Card Reader |
| 11 | CAMERA |

<Core Design>

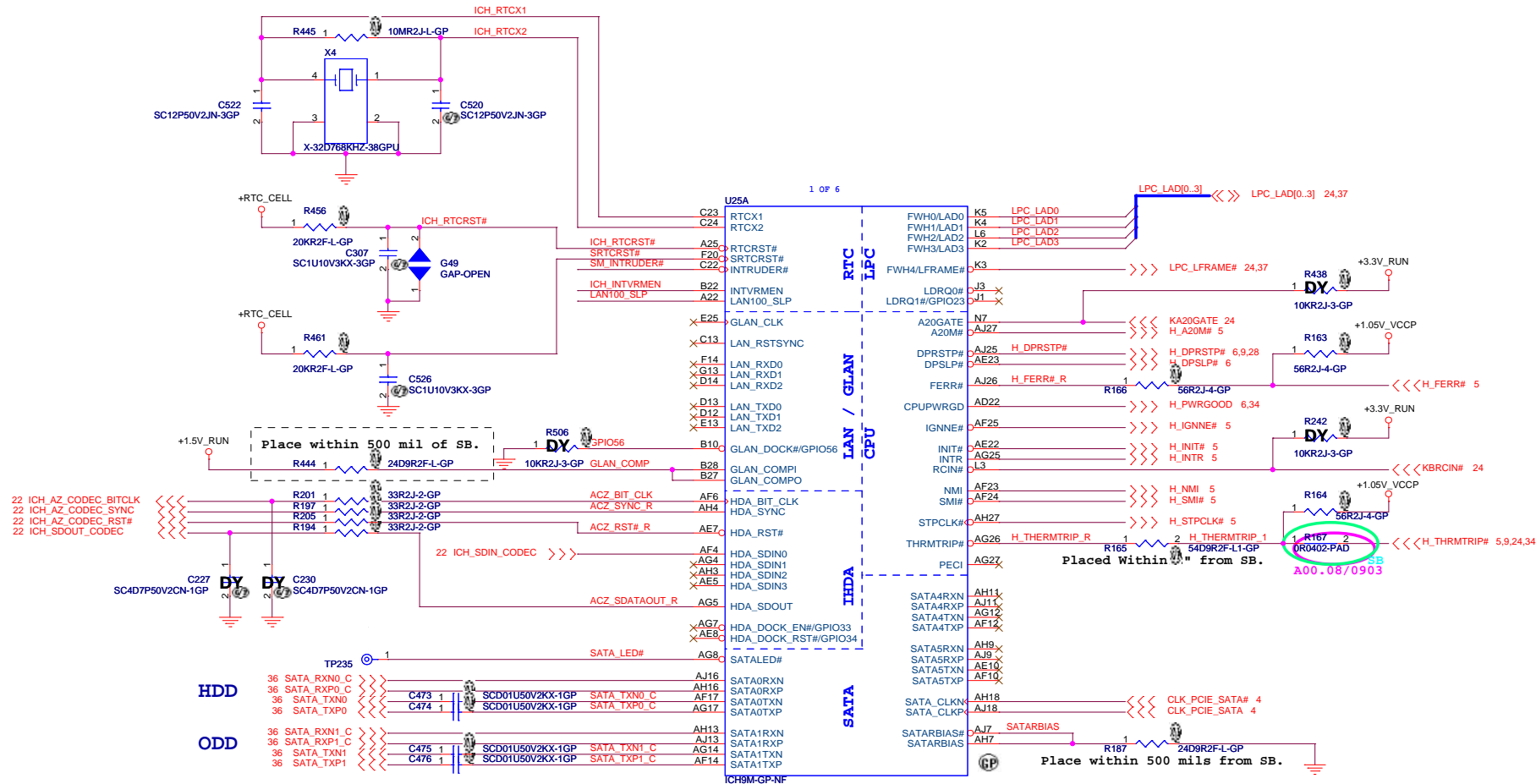
DELL Wistron Corporation
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File: **ICH9-PCI/PCIE/DMI/USB/GND(1/4)**
Size: Custom Document Number
Date: Monday, March 16, 2009 Sheet 16 of 58

Rev SB

DR2 17" UMA

SSID = ICH



HDD

ODD

| | |
|--|-------------------------|
| Integrated VccSus1_05, VccSus1_5, VccCl1_5 | |
| INTVRMEN | High=Enable Low=Disable |
| Integrated VccLan1_05VccCl1_05 | |
| LAN100_SLP | High=Enable Low=Disable |

<Core Design>

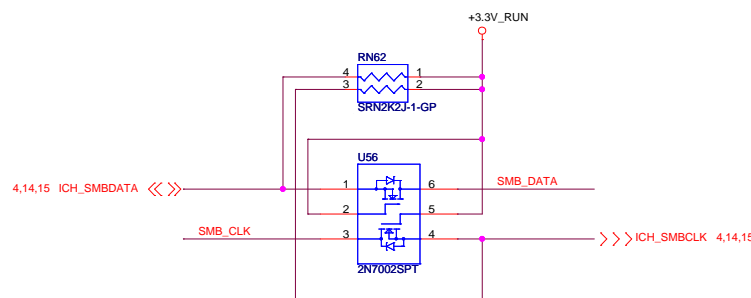
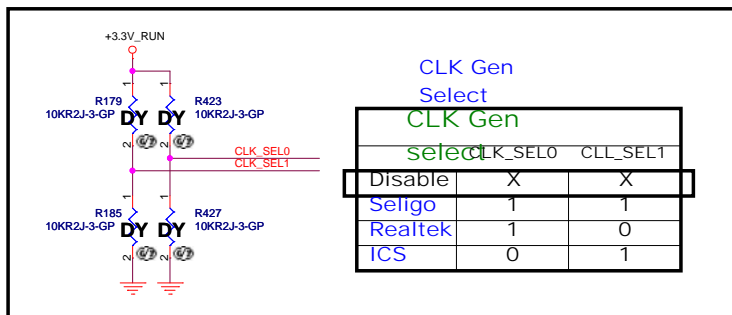
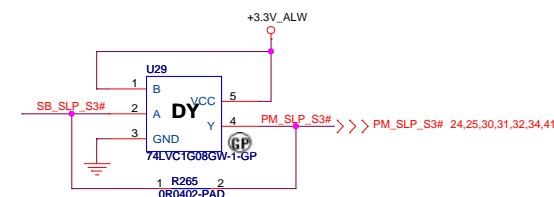
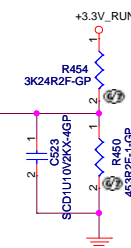
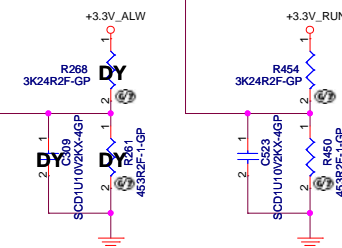
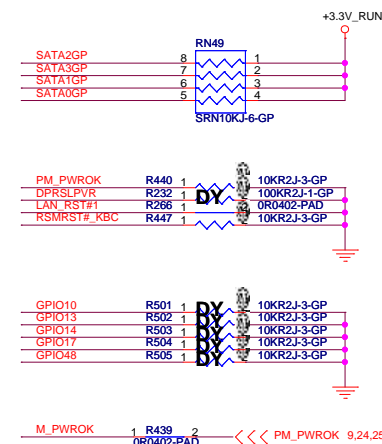
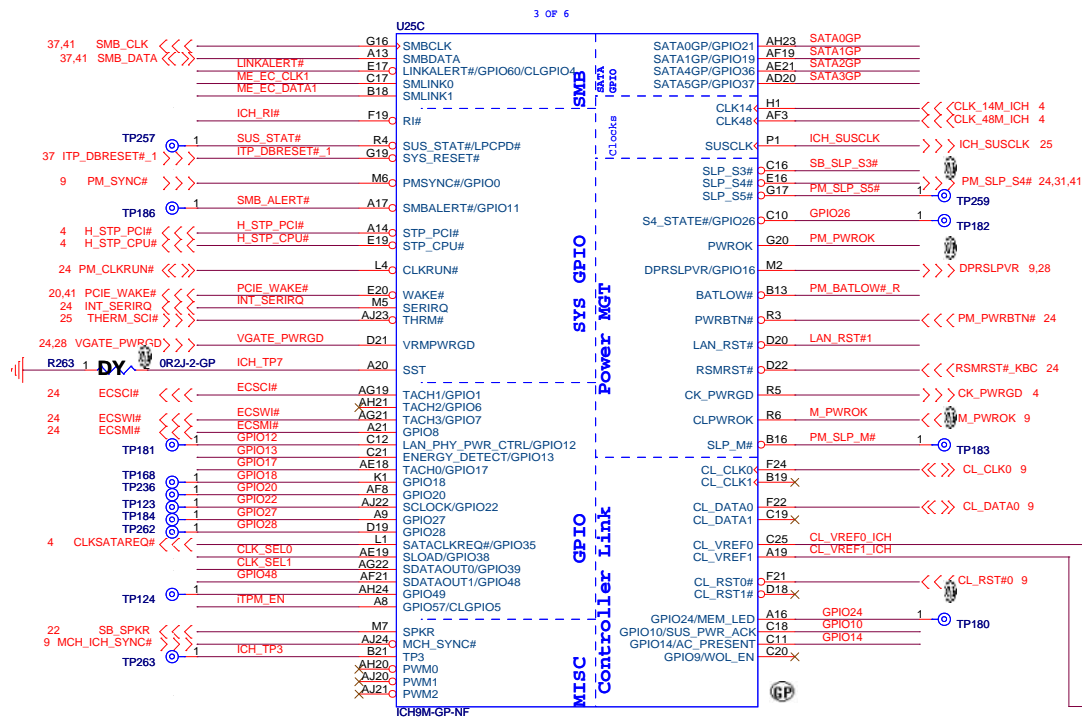
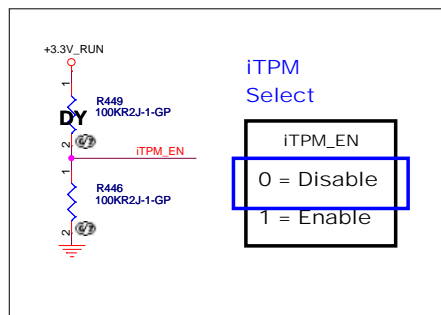
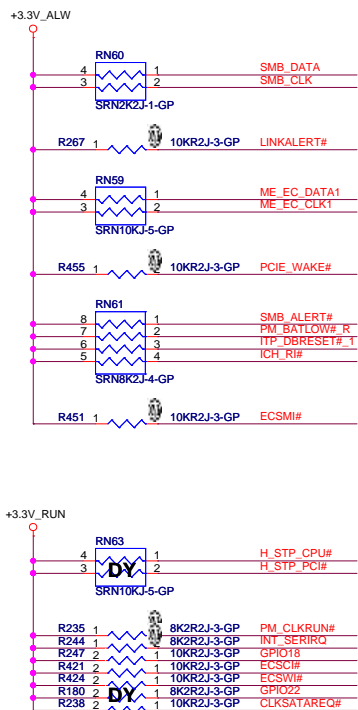
DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

File: **ICH9-LAN/HDA/SATA/LPC(2/4)**

Size: Custom Document Number: **DR2 17" UMA** Rev: SB

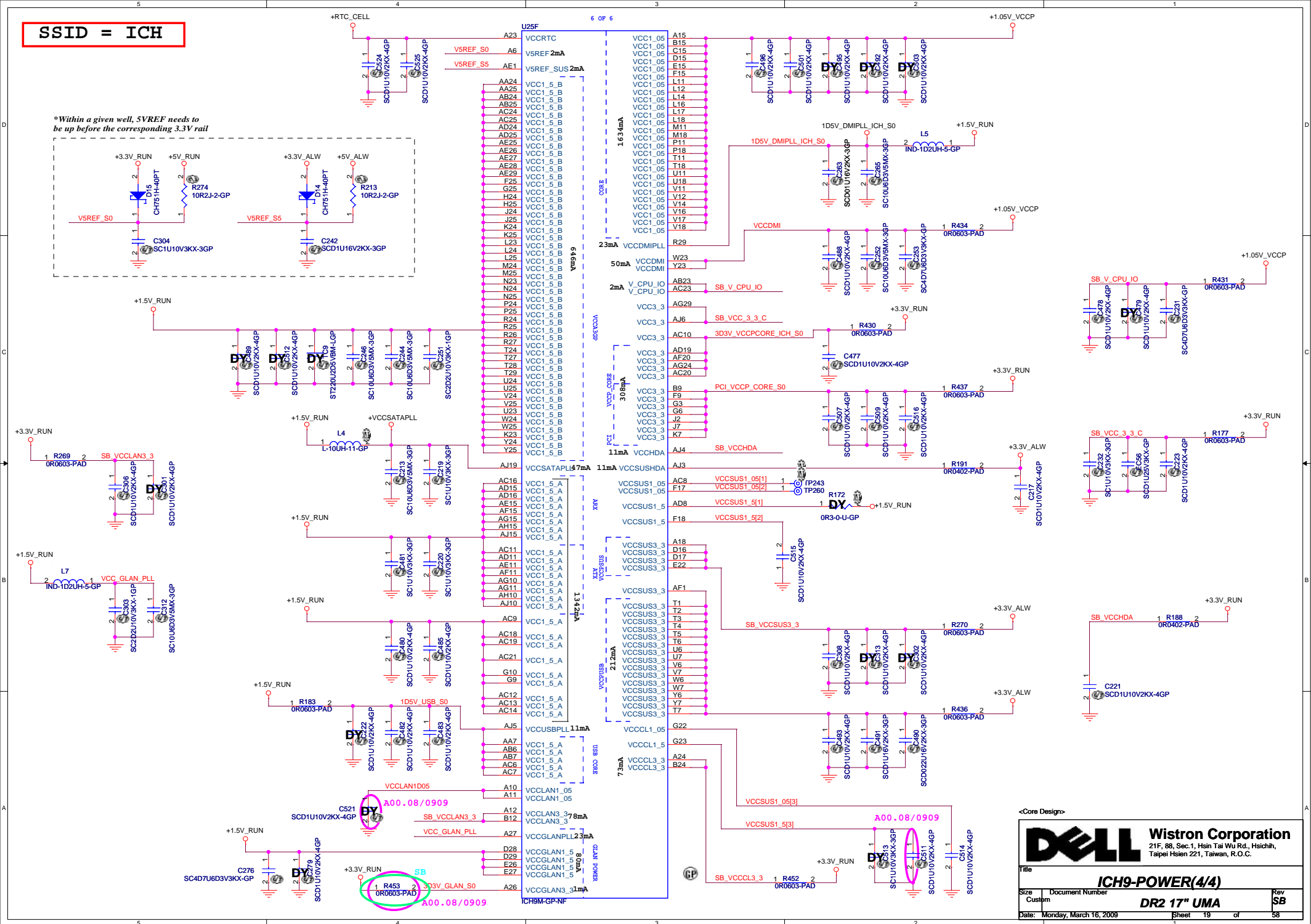
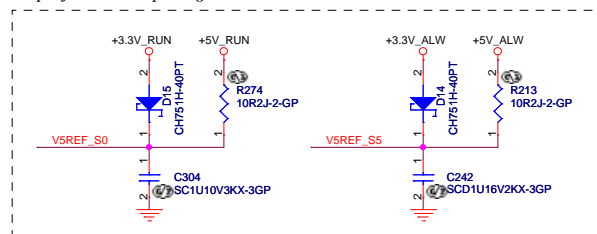
Date: Monday, March 16, 2009 Sheet 17 of 58

SSID = ICH



SSID = ICH

**Within a given well, 5VREF needs to be up before the corresponding 3.3V rail*

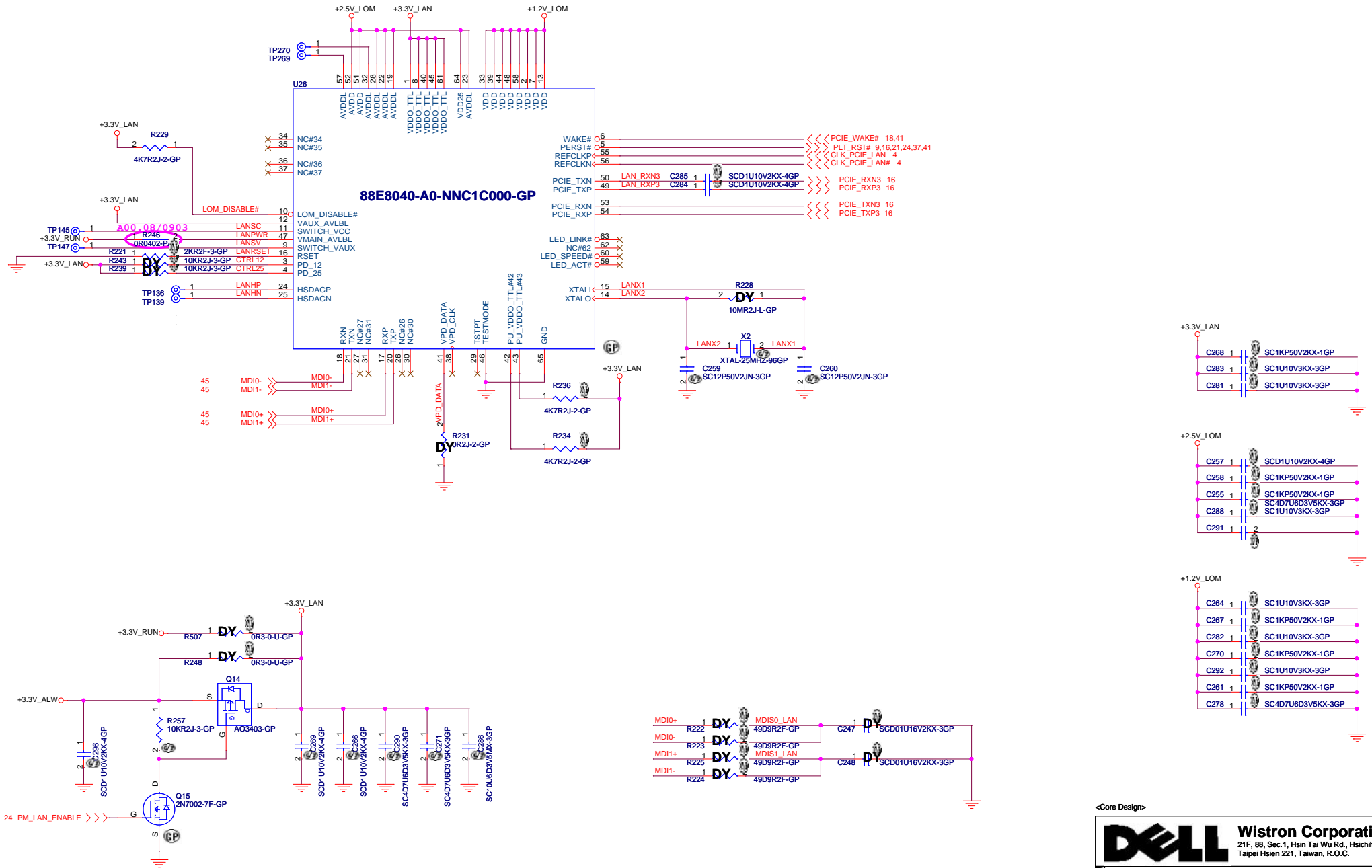


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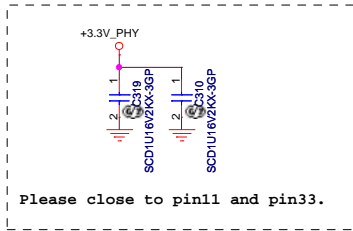
DELL **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | | |
|------------------------|------------------------|-------------|-----------|
| Title | | | |
| ICH9-POWER(4/4) | | | |
| Size | Document Number | | Rev |
| Custom | DR2 17" UMA | | SB |
| Date: | Monday, March 16, 2009 | Sheet 19 of | 58 |

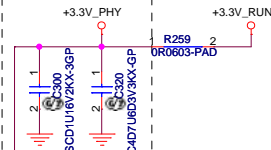
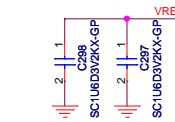
SSID = LOM



SSID = SDIO

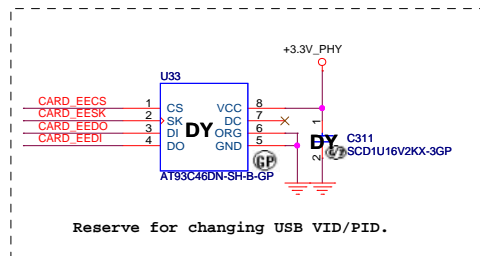
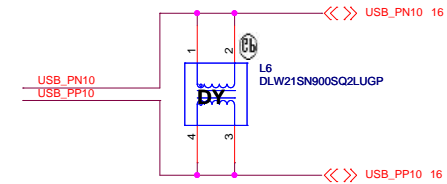
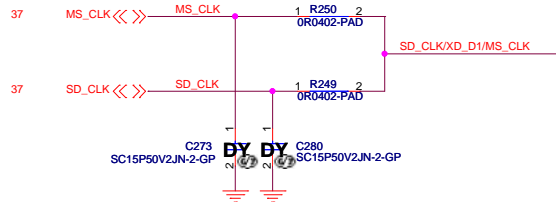
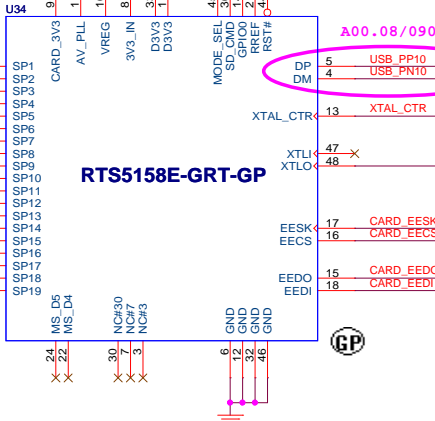


Please close to pin8.



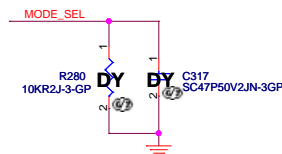
37 XD_CD#
37 SD_WP
37 SD_CD#
37 XD_D4/SD_DAT1
37 XD_D5/MS_BS
37 XD_D3/MS_D1
37 XD_D1/MS_D0
37 XD_D2/MS_D2
37 MS_INS#
37 XD_D7/MS_D3
37 SD_CLK/XD_D1/MS_CLK
37 XD_D0
37 XD_WP#
37 XD_RDY
37 SD_DAT3/XD_WE#
37 SD_DAT2/XD_RE#
37 XD_ALE
37 XD_CE#
37 XD_CLE

XD_CD#
SD_WP
XD_D4/SD_DAT1
XD_D5/MS_BS
XD_D3/MS_D1
XD_D1/MS_D0
XD_D2/MS_D2
MS_INS#
XD_D7/MS_D3
SD_CLK/XD_D1/MS_CLK
XD_D0
XD_WP#
XD_RDY
SD_DAT3/XD_WE#
SD_DAT2/XD_RE#
XD_ALE
XD_CE#
XD_CLE



Power mode select

No staff R and C for power saving mode.



<Core Design>

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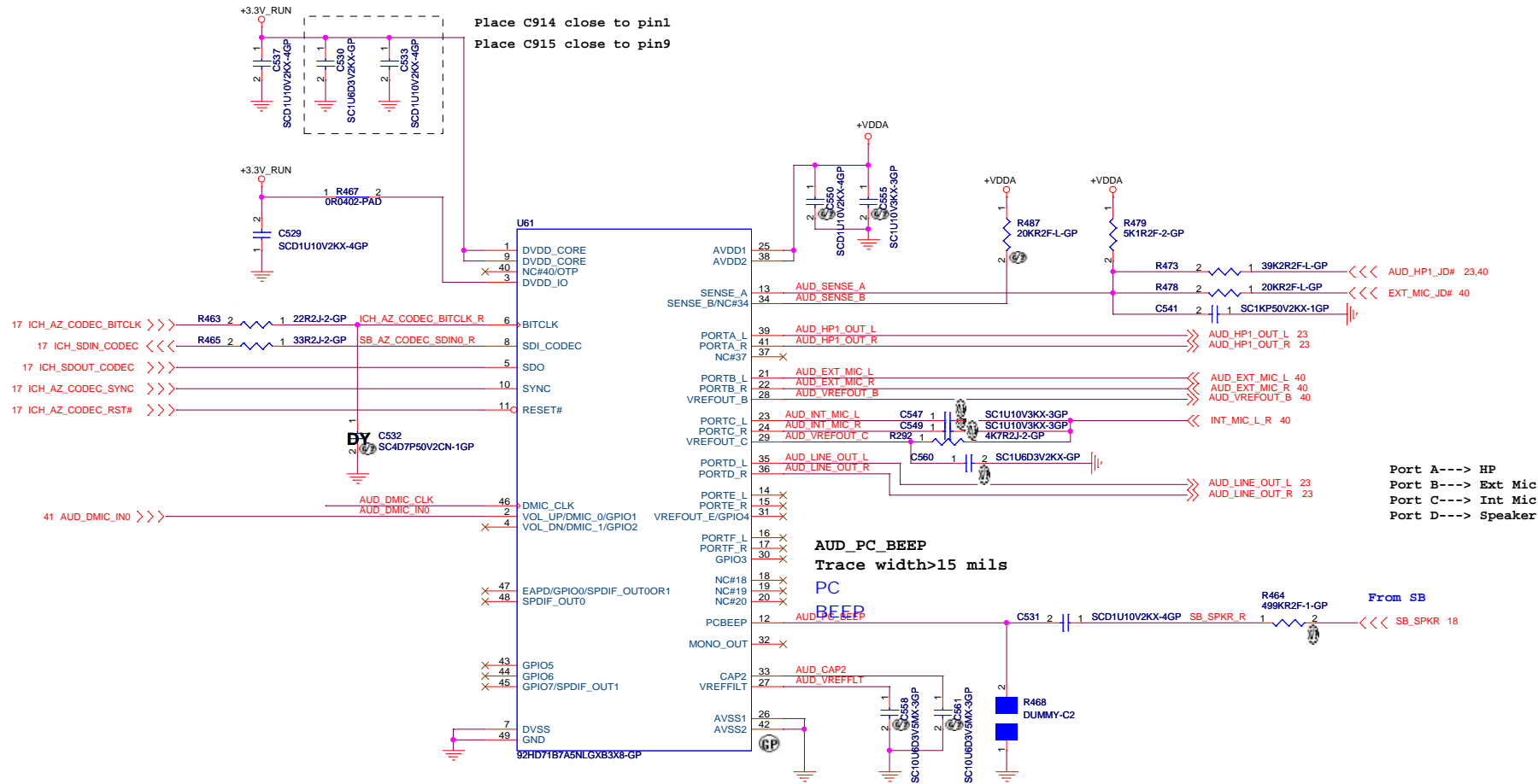
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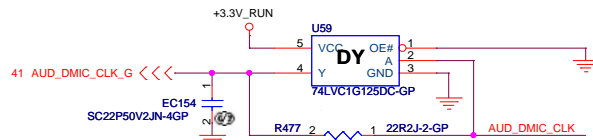
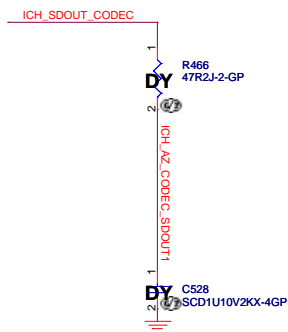
Date: Monday, March 16, 2009 Sheet 21 of 58

Rev: **SB**

SSID = AUDIO



Azalia I/F EMI

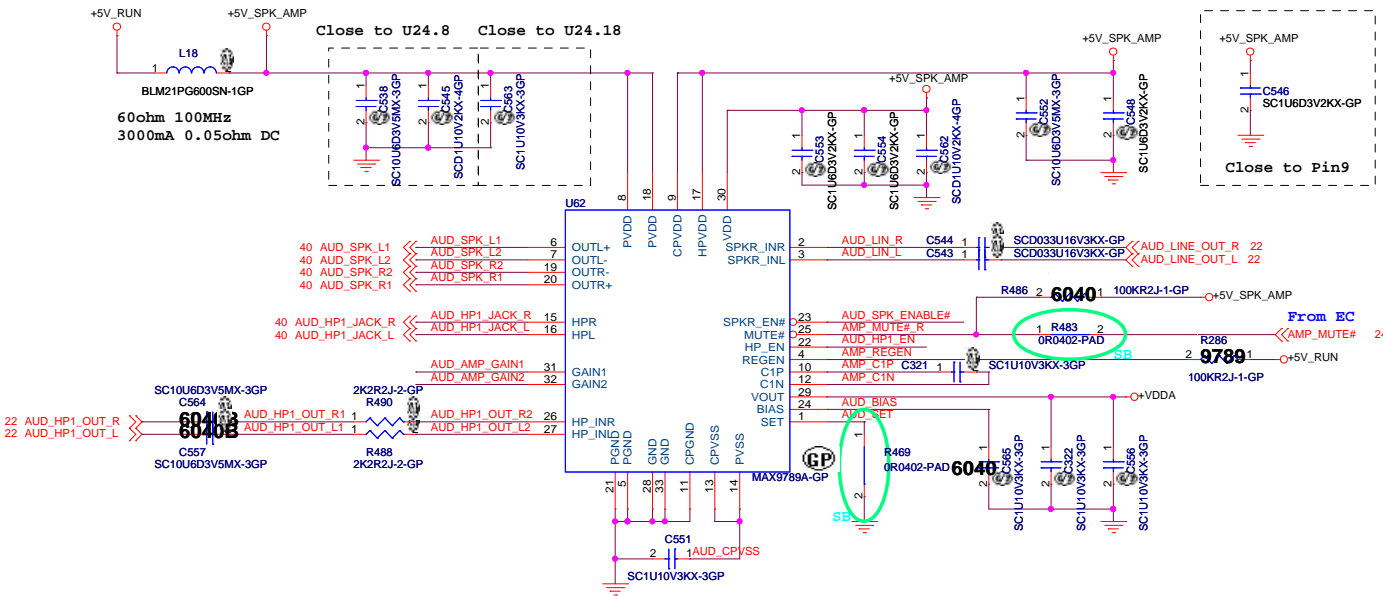


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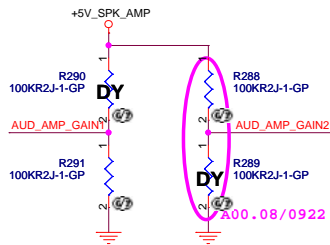


| | | | | |
|--------|------------------------|-----------------|----|-------|
| File | | Document Number | | Rev |
| CUSTOM | | DR2 17" UMA | | SB |
| Date: | Monday, March 16, 2009 | Sheet | 22 | of 58 |

SSID = AUDIO

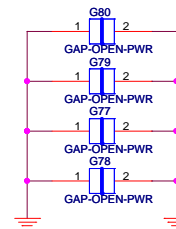


GAIN SETTING

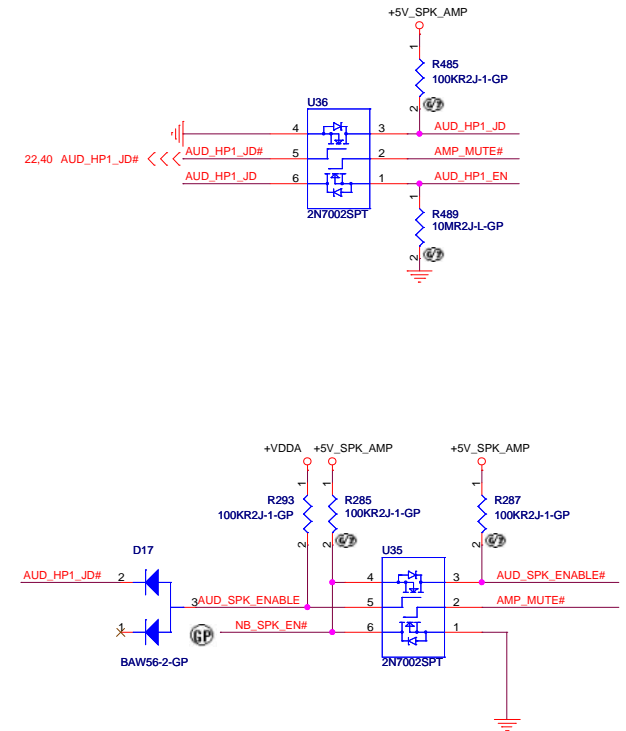


| GAIN1 | GAIN2 | GAIN |
|-------|-------|--------|
| 0 | 0 | 6dB |
| 0 | 1 | 10dB |
| 1 | 0 | 15.6dB |
| 1 | 1 | 21.6dB |

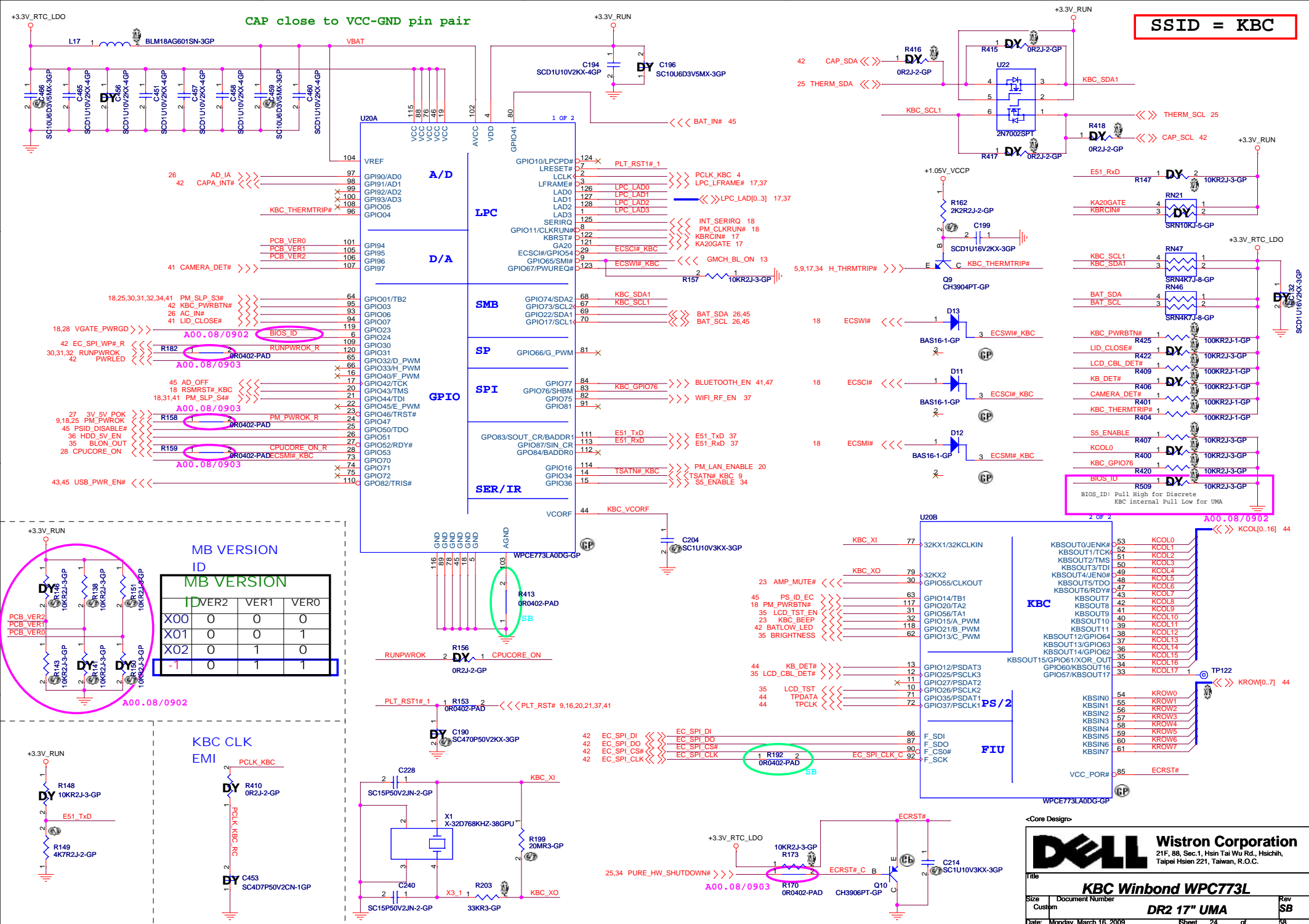
| | Main source | Second source |
|------|-------------------------|-------------------------|
| | TPA6040A (74.06040.013) | MAX9789A (74.09789.013) |
| R486 | 100K | No ASM |
| R483 | No ASM | 0 Ohm |
| R469 | No ASM | 0 Ohm |
| R286 | No ASM | 100K |
| C535 | 0.033uF | No ASM |
| C566 | 0.033uF | No ASM |
| C565 | 1uF | No ASM |
| C567 | No ASM | 0.1uF |
| C564 | 10uF | 2.2uF |
| C557 | 10uF | 2.2uF |



Signal inverter for speaker shutdown



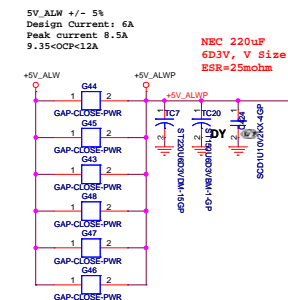
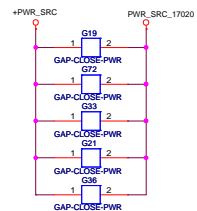
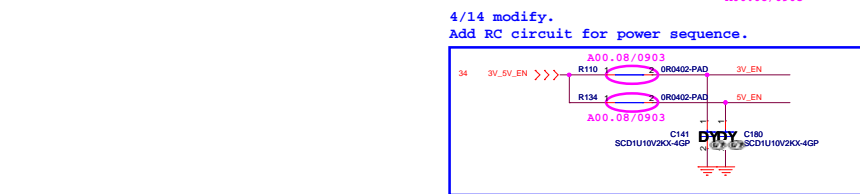
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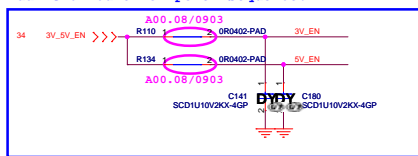
SSID = Thermal



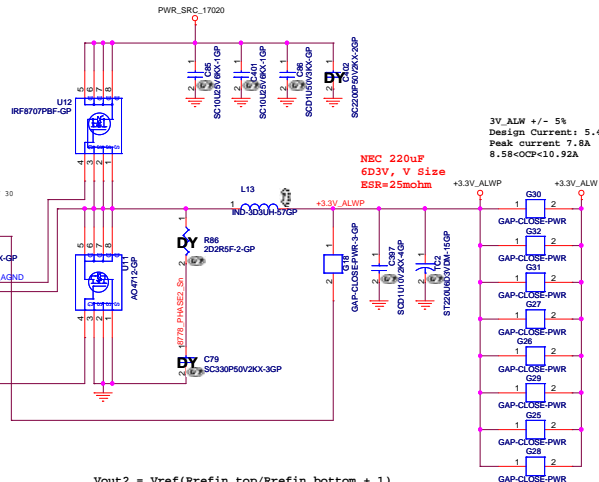
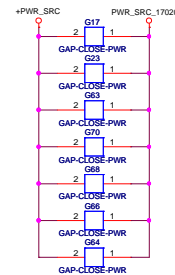
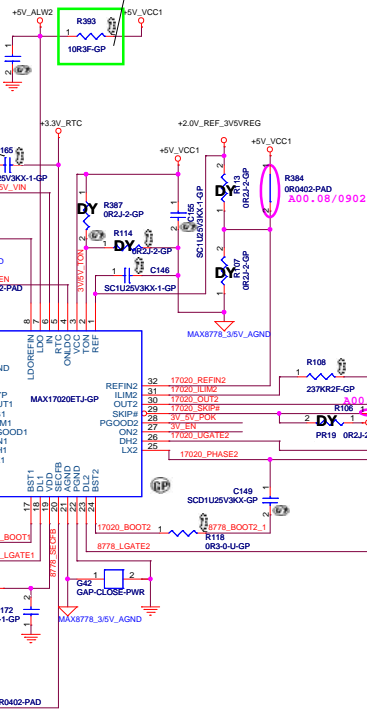

```
SSID = PWR.Plane.Regulator_3p3v5v
```


$$V_{out1} = 0.7(R_{top}/R_{bottom} + 1)$$


4/14 modify.
Add RC circuit for power sequence.

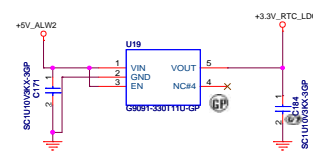
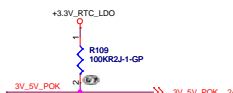


No Install for ISL6236
Install 10 ohm for MAX8778



```
Vout2 = Vref(Rrefin_top/Rrefin_bottom + 1)
```

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMC0637R3R3M1 CYNTEC DCR 28-30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: 220U 6.3V PSLV02J227M(25) 25mohm 2.236Arms NEC_TOKIN/77.C12271.00L
O/P cap: 150U 6.3V PSLB20J157M(45) 45mohm 1.374rms NEC_TOKIN/77.C1571.09L
H/S: IRF8702 SO-8 / 14.2mohm/17.5mOhm@4.5Vgs/ 84.08707.037
L/S: FDS4712 SO-8 / 15mohm/18mOhm@4.5Vgs/ 84.04712.037



```
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMC062373R3M CNYTEC DCR 28~30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: 220U 6.3V PSLV03J2272M(25) 25mohm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 150U 6.3V PSLB220J157M(45) 45mOhm 1.374rms NEC_TOKIN/77.C1571.09L
H/S: IRF8707 SO-8/ 14.2mohm/17.5mOhm@4.5Vgs/ 84.08707.037
L/S: FDS4712 SO-8/ 15mohm/18mOhm@4.5Vgs/ 84.04712.037
```

| | | | |
|----------------|---------------------|-----------------|-----------------------|
| SKIPSEL | GND | Open/REF (2V) | High (VCC or 3.3V) |
| Operating Mode | pulse-skipping mode | ultrasonic mode | forced-PWM operation |

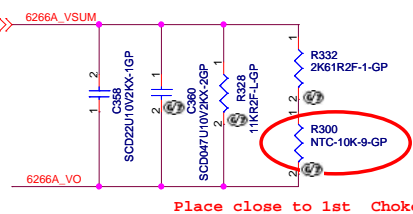
| TONSEL | GND | Open (REF) | High (VCC) |
|----------|--------|------------|------------|
| CH1 Freq | 400kHz | 400kHz | 200kHz |
| CH2 Freq | 500kHz | 300kHz | 300kHz |

| | | | |
|-------------------|---------------|---------------|---------------------|
| LDOREFIN | GND | VCC | VLDOREFIN = 0.5V |
| Operating Mode | 4.90/5.0/5.10 | 3.23/3.3/3.37 | 0.96/1.0/1.04 |

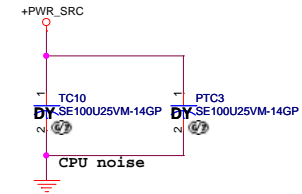
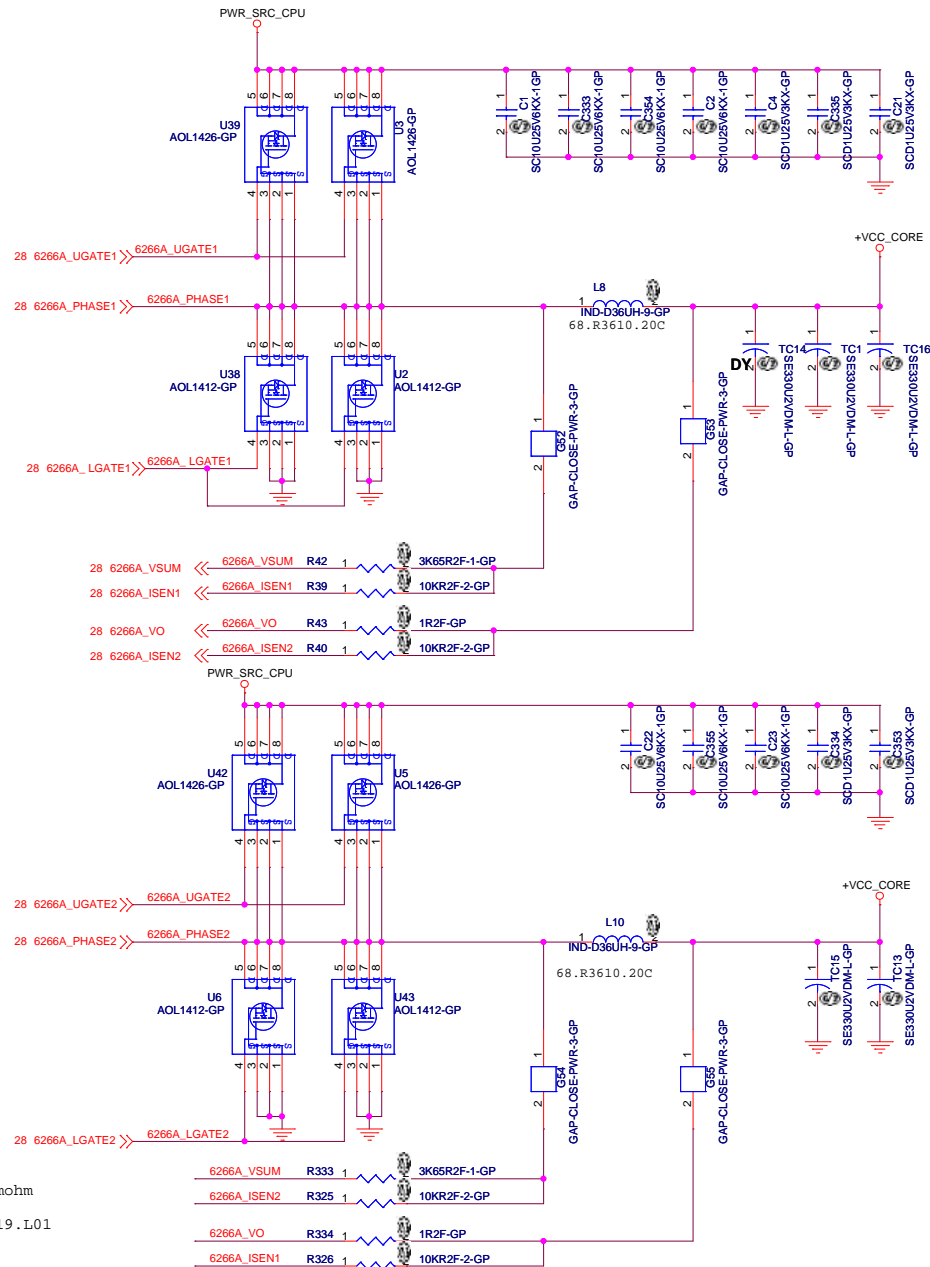
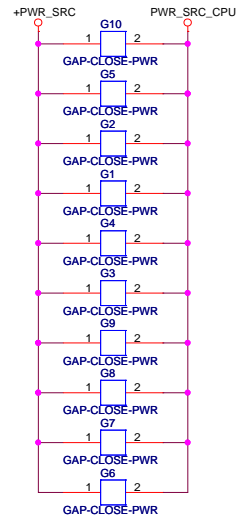
| | | | |
|----------------|------------------|------------------|--|
| FB1 | GND | VCC | |
| Operating Mode | 4.925/5.00/5.075 | 1.482/1.50/1.518 | |

| | | | |
|----------------|------------------|--------------------|--|
| REFIN2 | 5V | RTC (3.3V) | |
| Operating Mode | 3.255/3.30/3.345 | 1.038/1.050 /1.062 | |

```
SSID = CPU.Regulator
```



```
SSID = CPU.Regulator
```



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MNR05J CYNTEC DCR 1.05(+5%~-5%)mohm
Isat =60Arms 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S: AOL1426 PowerPAK/ 1.2mohm/12.5mOhm@4.5Vgs/84.01426.037
L/S: AOL1412 PowerPAK/ 3.8mohm/4.65mOhm@4.5Vgs/ 84.01412.037

<Core Design>

DELL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU VCORE POWER(2/2)

| | |
|------|--|
| Size | |
|------|--|

Document Number

DR2 17" UMA

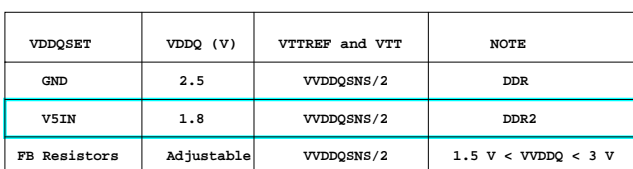
Date: Monday, March 16, 2009

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Rev

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TI TPS51116 for 1.8V and 0.9V



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCM0637-1R5M(Cyntec DCR:14~15mohm Isat =18Arms 68.1R510.10K
O/P cap: 330U 2.5V PSLV0C3377M(15) 15mohm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: FDS8880 SO-8/9.6mohm/ 12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->400KHz

A00.08/0903

18,24,25,30,32,34,41 PM_SLP_S3#

18,24,41 PM_SLP_S4#

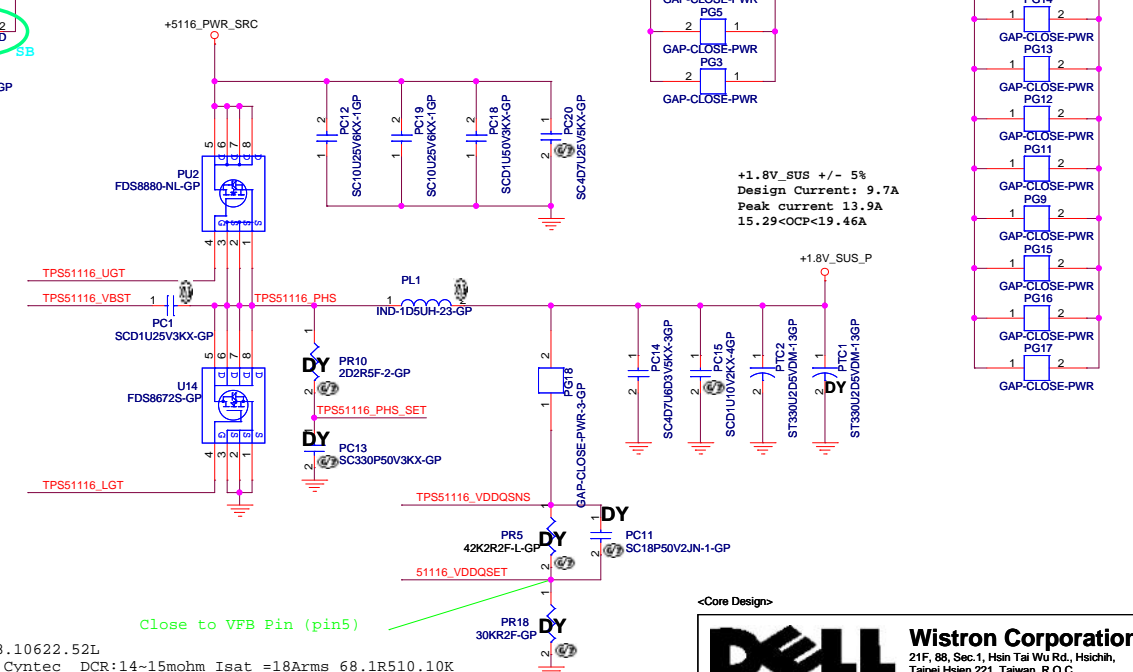
PR9 1 2 OR402-PAD

PR8 1 2 OR2J-2-GP

OD9V_EN

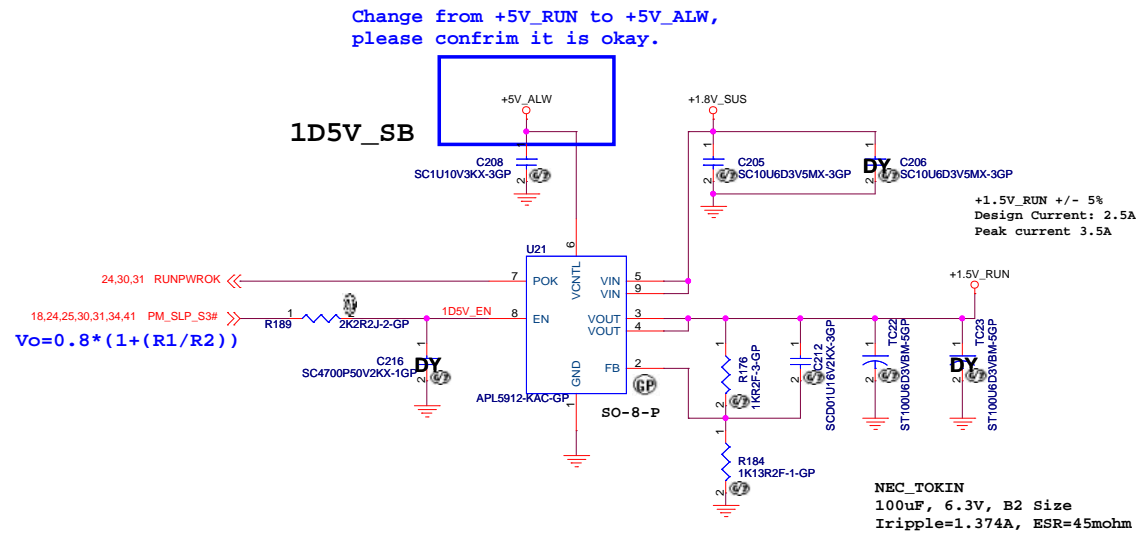
10k

CD89 SCD1U10V2KX-4GP



| | | | |
|----------------------------|------------------------|--|-----------|
| <Core Design> | | | |
| DELL | | Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsiang Z21, Taiwan, R.O.C. | |
| Title | | | |
| | | DC to DC 1.8V/0.9V | |
| Size | Document Number | | Rev |
| Custom | | DR2 17T | SA |
| Date: | Monday, March 16, 2009 | Sheet | 31 of 58 |

SSID = PWR.Plane.Regulator_1p5v



<Core Design>




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| | | | |
|---------------|------------------------|-------------|-----|
| Title | | | |
| DC to DC 1.5V | | | |
| Size | Document Number | | Rev |
| Custom | DR2 17" UMA | | SB |
| Date: | Monday, March 16, 2009 | Sheet 32 of | 58 |

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

File

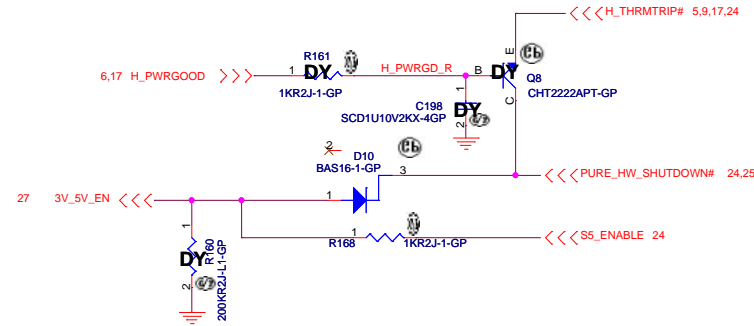
Size
Custom

Document Number
DR2 17" UMA

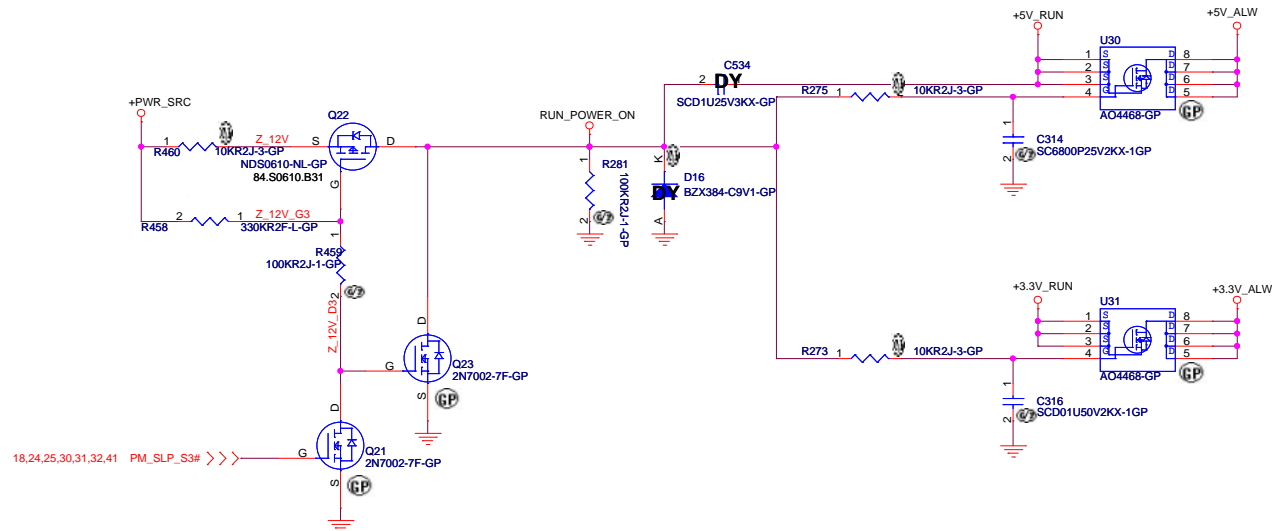
Rev
SB

Date: Monday, March 16, 2009Sheet 33 of 58

SSID = Reset.Suspend



Run Power



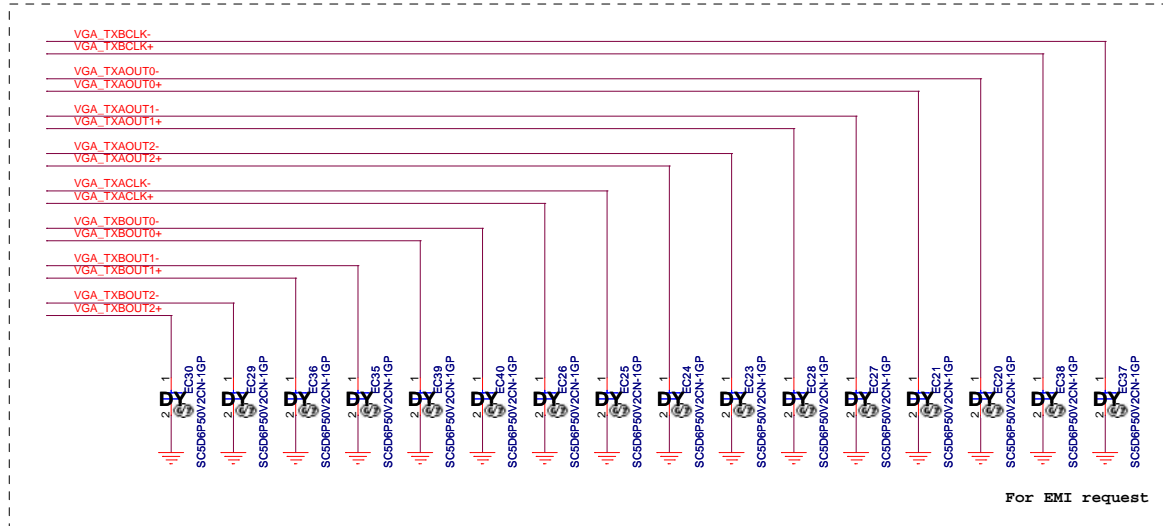
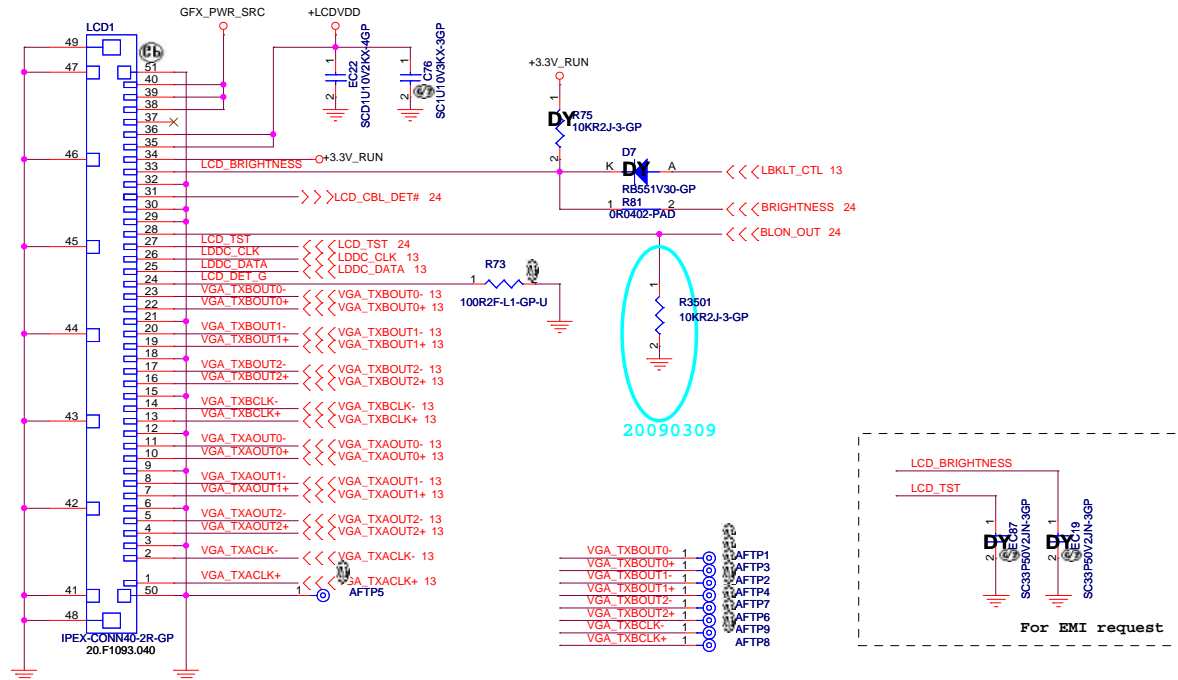
<Core Design>



| | | | |
|-------|------------------------|-----------------|----------|
| File | Power Plane Enable | | |
| Size | Custom | Document Number | Rev |
| | | DR2 17" UMA | SB |
| Date: | Monday, March 16, 2009 | Sheet | 34 of 58 |

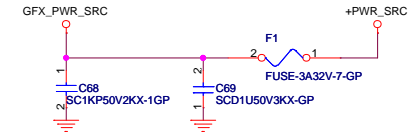
SSID = VIDEO

LVDS CONNECTOR



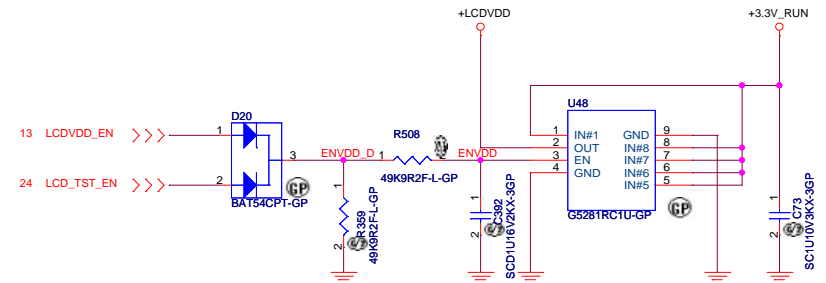
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



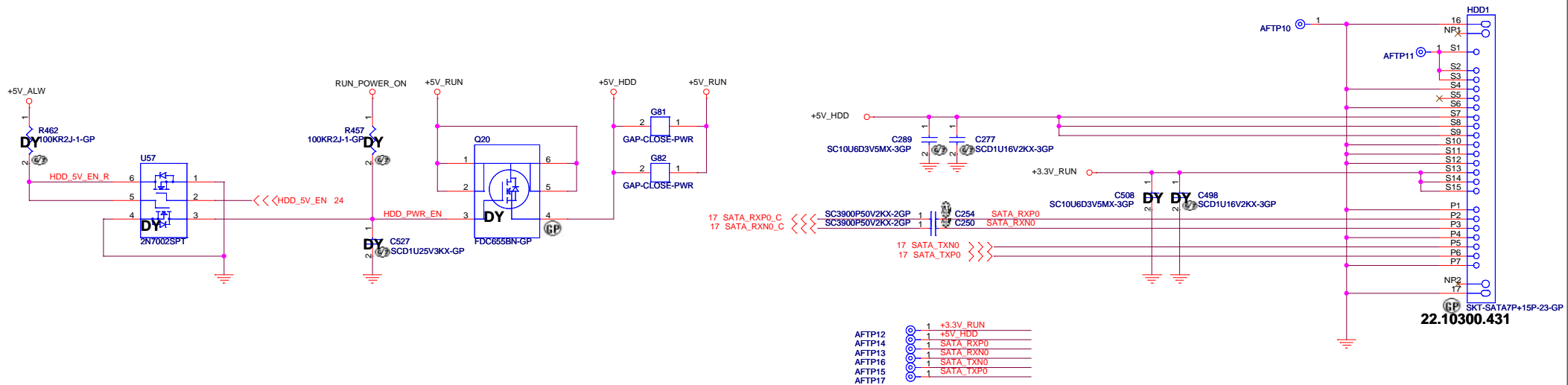
<Core Design>

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| | | | |
|------------------------------|-----------------|-------------------------------|----|
| Title | | LCD/Inverter Connector | |
| Size | Document Number | Rev | SB |
| Custom | | DR2 17" UMA | |
| Date: Monday, March 16, 2009 | Sheet 35 | of | 58 |

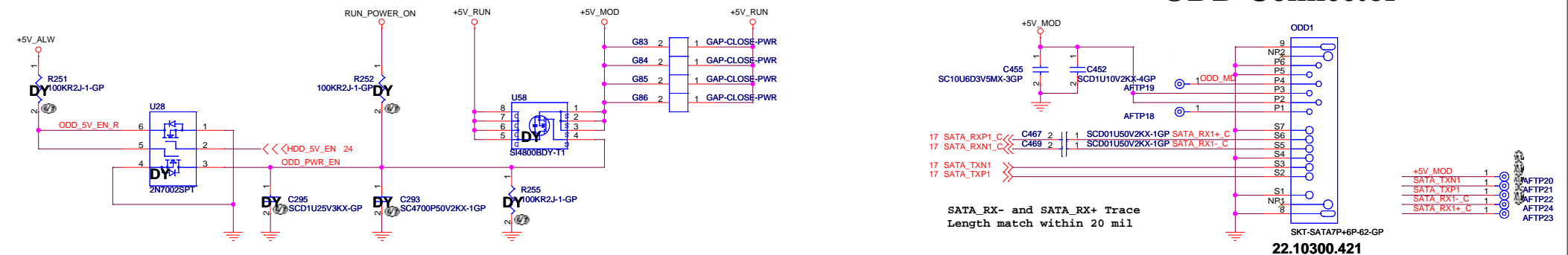
SSID = SATA

SATA HDD Connector



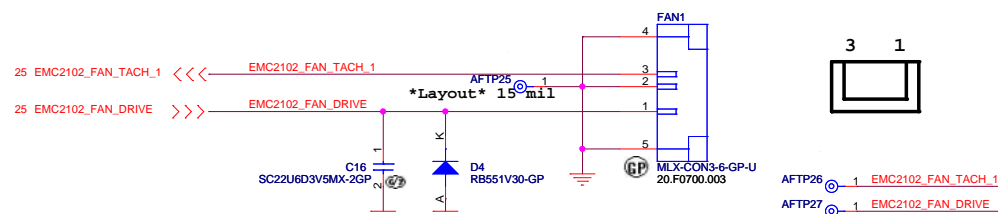
SSID = SATA

ODD Connector



SSID = Thermal

Fan Connector



<Core Design>

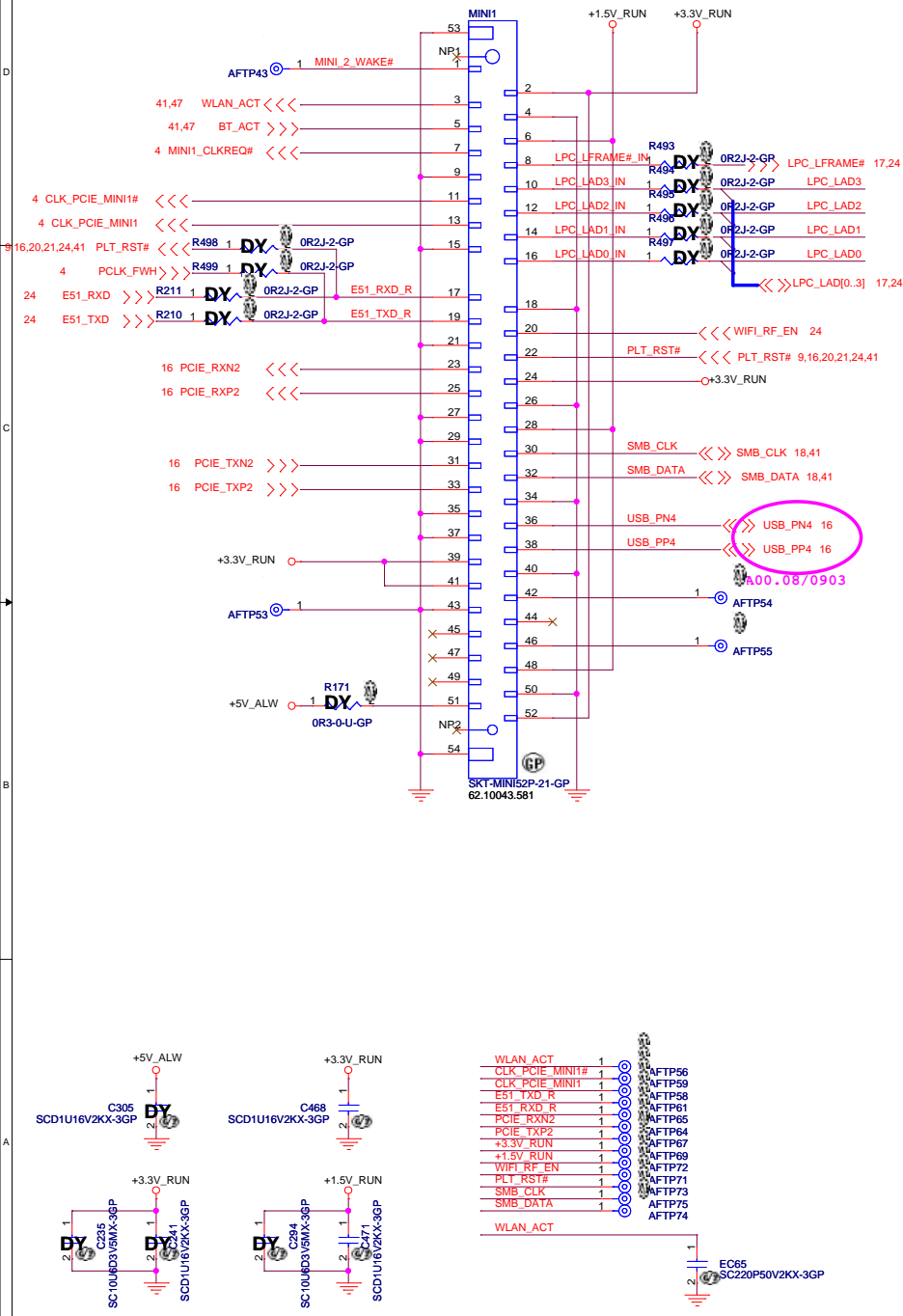


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| | | | |
|--------------------|------------------------|--|----------------|
| Title | | | |
| HDD/ODD/FAN | | | |
| Size | Document Number | | Rev |
| Custom | DR2 17" UMA | | SB |
| Date: | Monday, March 16, 2009 | | Sheet 36 of 58 |

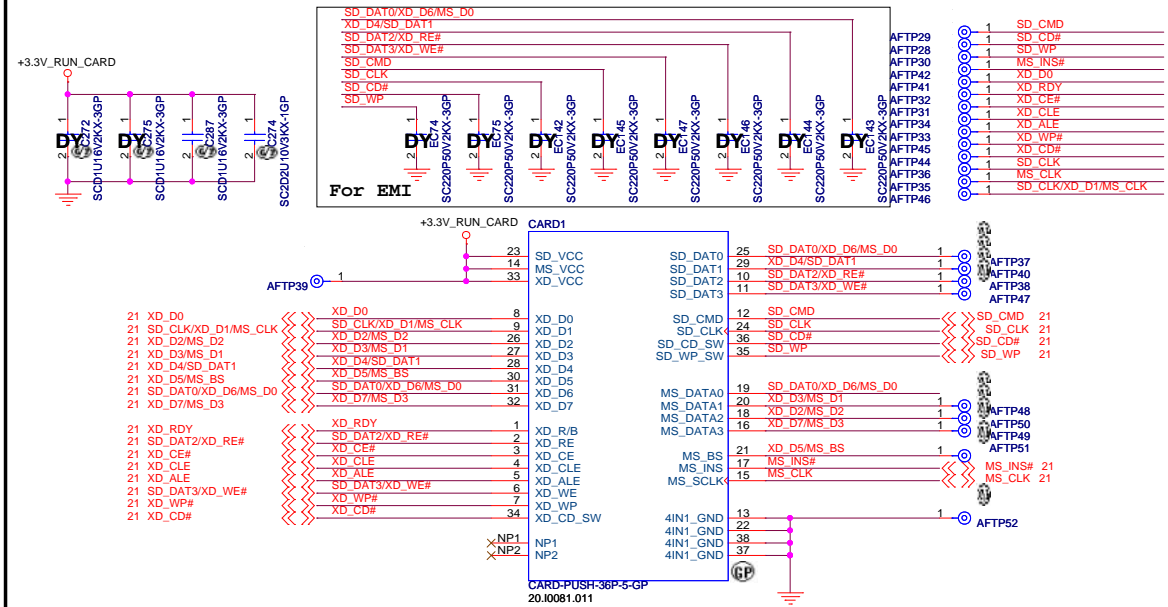
SSID = Wireless

Mini Card Connector(802.11a/b/g)



SSID = SDIO

SD/XD/MS Card Reader




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<Core Design>

| | | | |
|---|---------------------------------------|---|------------------|
|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | MINICARD(WWAN) | |
| Size Custom | Document Number DR2 17" UMA | | Rev SB |
| Date: Monday, March 16, 2009 | | Sheet 38 | of 58 |

(Blanking)

<Core Design>



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File

MINICARD(WPAN)

Size
Custom

Document Number
DR2 17" UMA

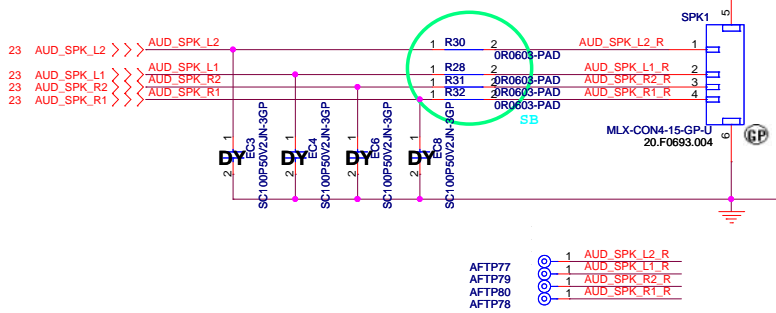
Rev
SB

Date: Monday, March 16, 2009

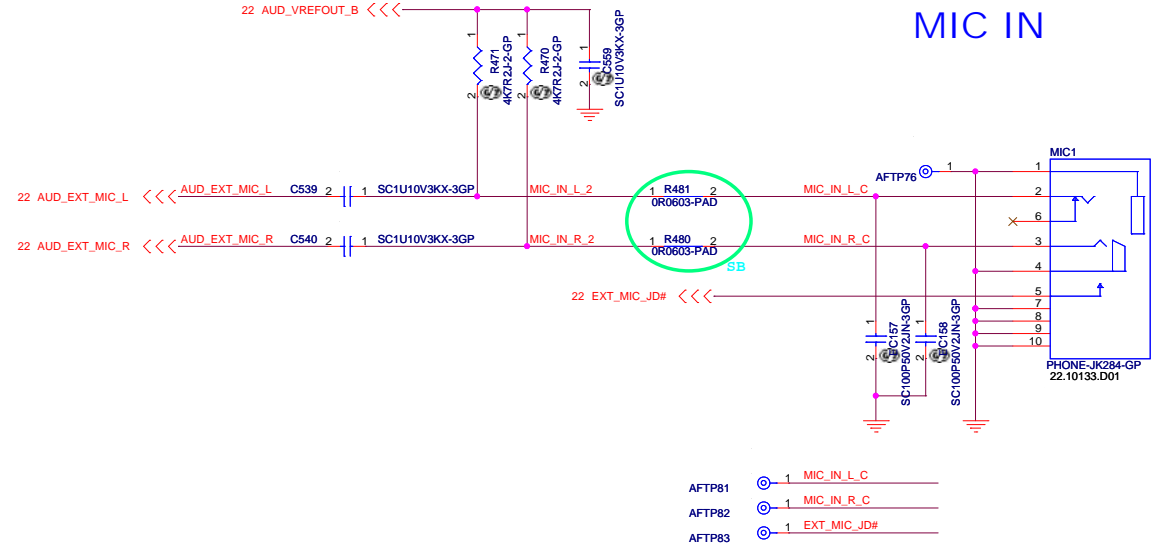
Sheet 39 of 58

SSID = AUDIO

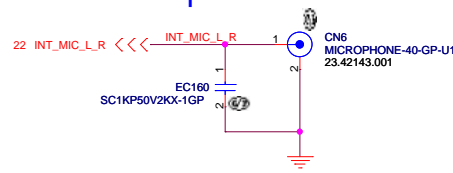
Speaker Connector



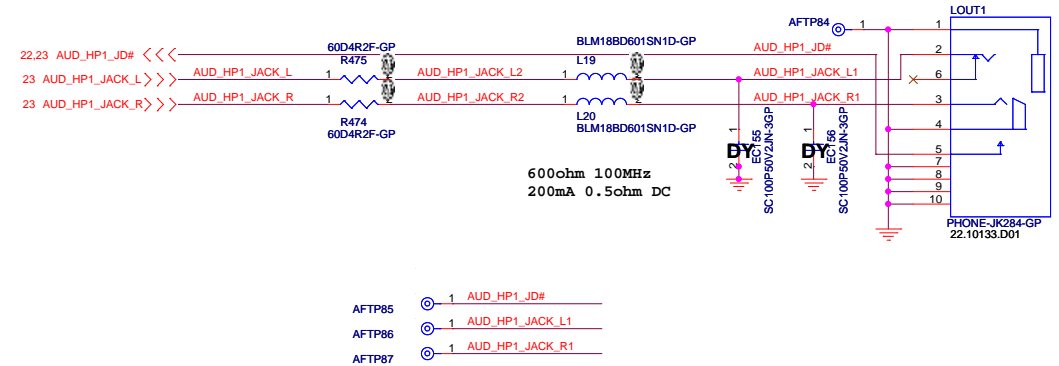
MIC IN



Internal Microphone



LINE1 OUT



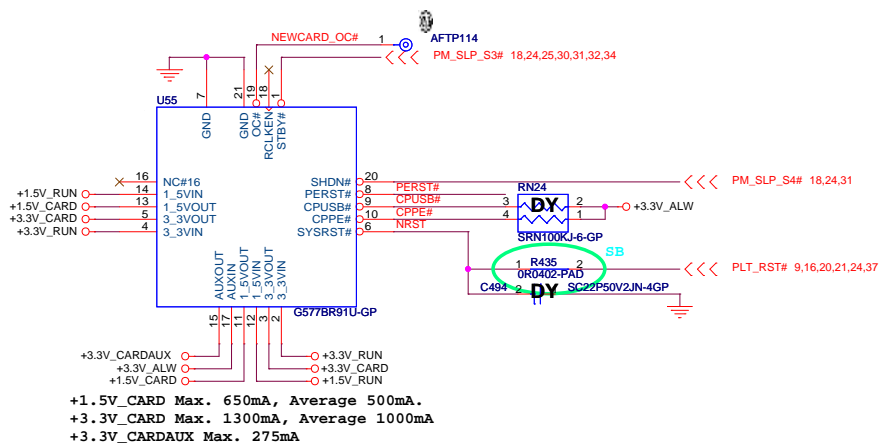
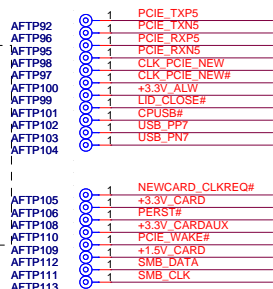
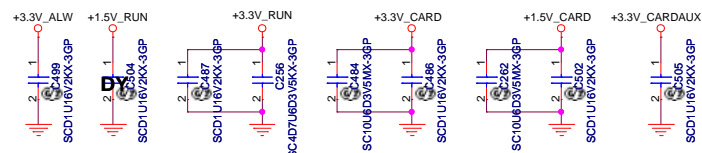
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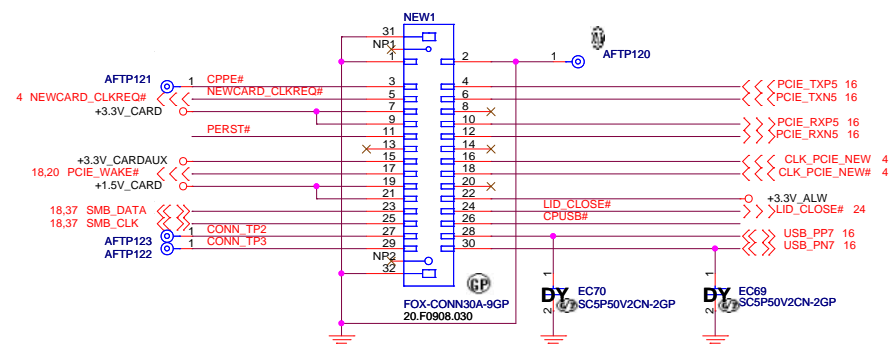
| | | | |
|--------|------------------------|------------|----------|
| File | | Audio Jack | |
| Size | Document Number | Rev | SB |
| Custom | DR2 17" UMA | | |
| Date: | Monday, March 16, 2009 | Sheet | 40 of 58 |


```
SSID = ExpressCard
```

Place them Near to Chip

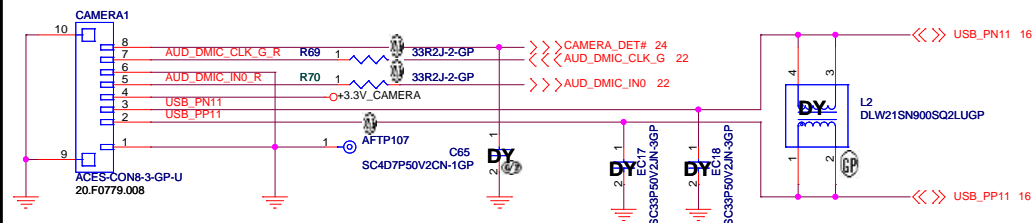


New Card Connector

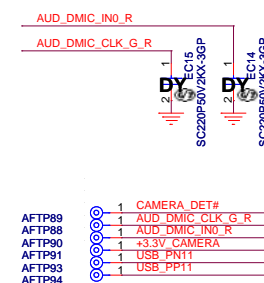
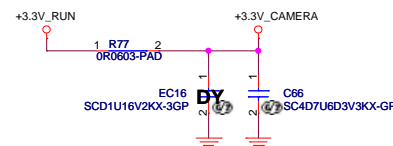


```
SSID = User.Interface
```

Camera Connector

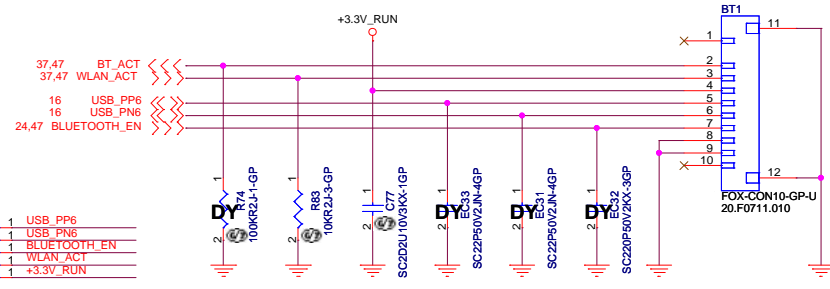


Digital Mic Power



```
SSID = User.Interface
```

Bluetooth Module conn.



<Core Design>

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Title

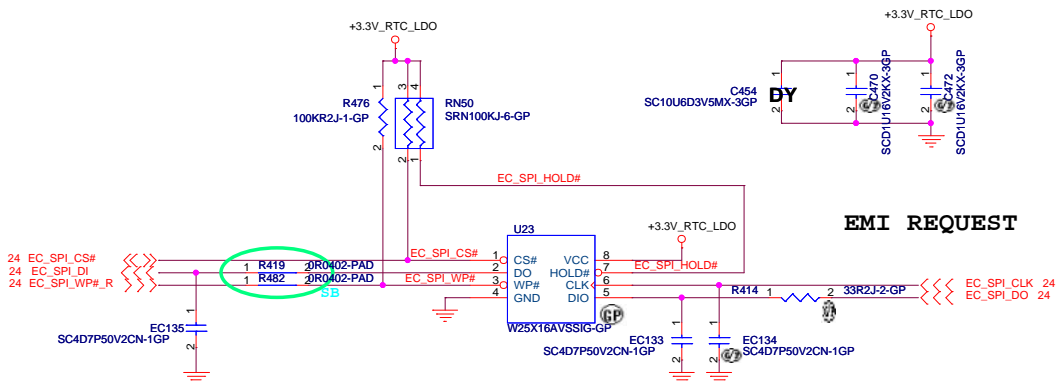
Bluetooth/CAM/New Card

| | | |
|--------|--------------------|-----------|
| Size | Document Number | Rev |
| Custom | DR2 17" UMA | SB |

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SPI FLASH ROM (16M bits)

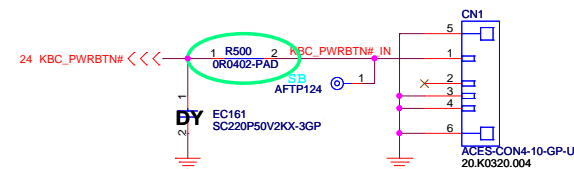
SSID = Flash.ROM



EMI REQUEST

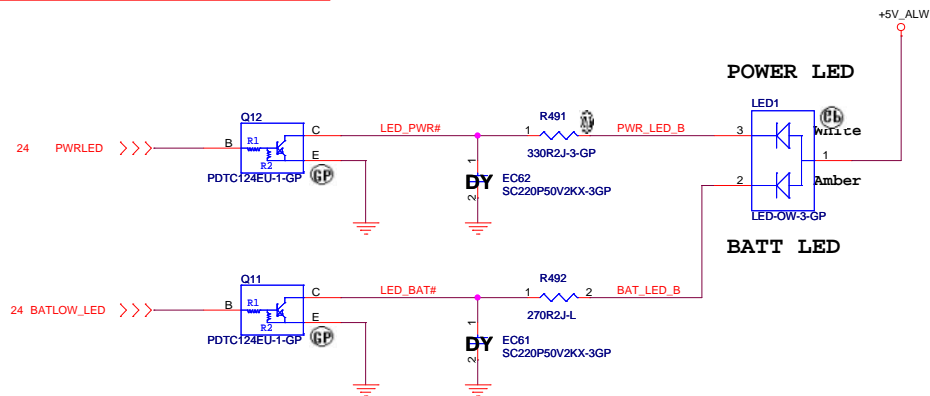
SSID = User.Interface

Power Dash Board to Board CONN



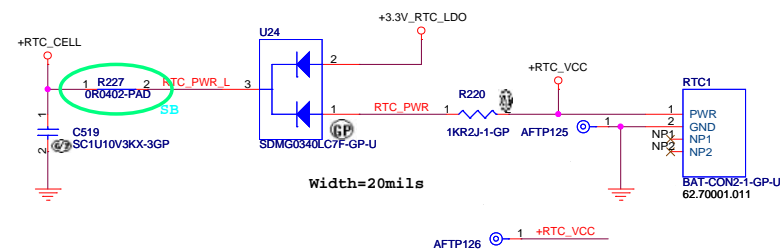
SSID = User.Interface

Power/Battery LED



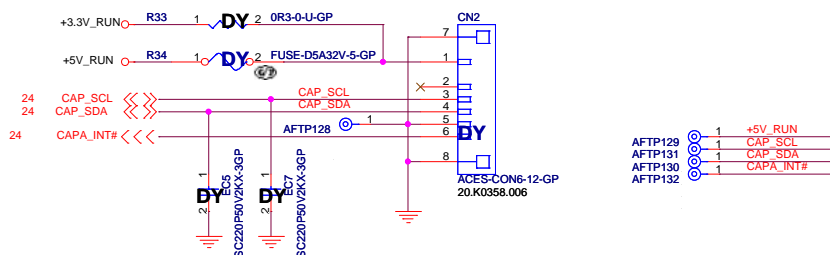
SSID = RBATT

RTC Connector



SSID = User.Interface

Capacitive Button



<Core Design>

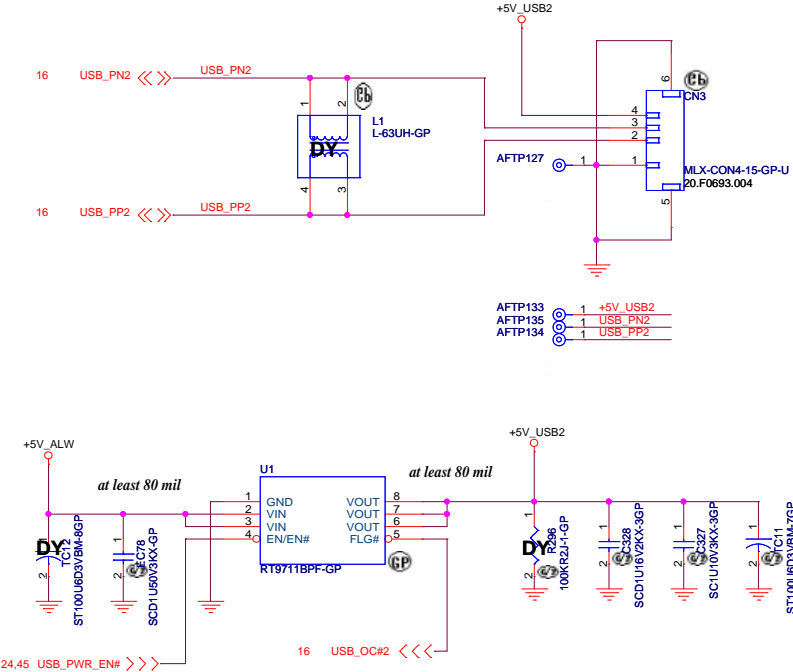


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| | | | |
|--------|----------------------------|-------|----------|
| File | FWH/LED/Power Dash/RTC/Cap | Rev | SB |
| Size | Document Number | | |
| Custom | DR2 17" UMA | | |
| Date | Monday, March 16, 2009 | Sheet | 42 of 58 |

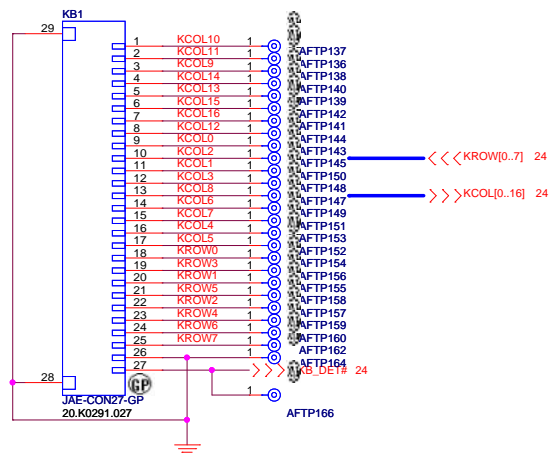
SSID = USB

Right USB Port CONN



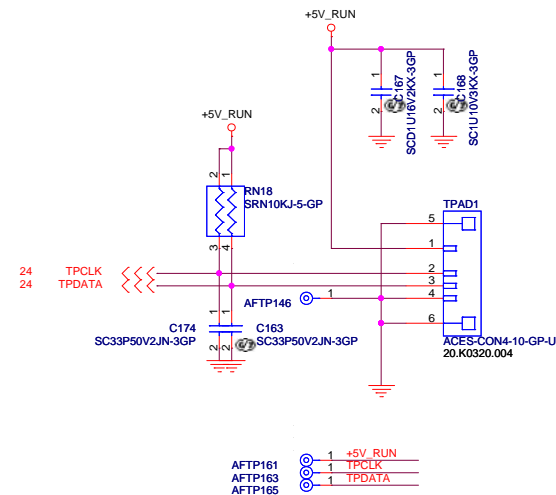
SSID = KBC

Internal KeyBoard Connector

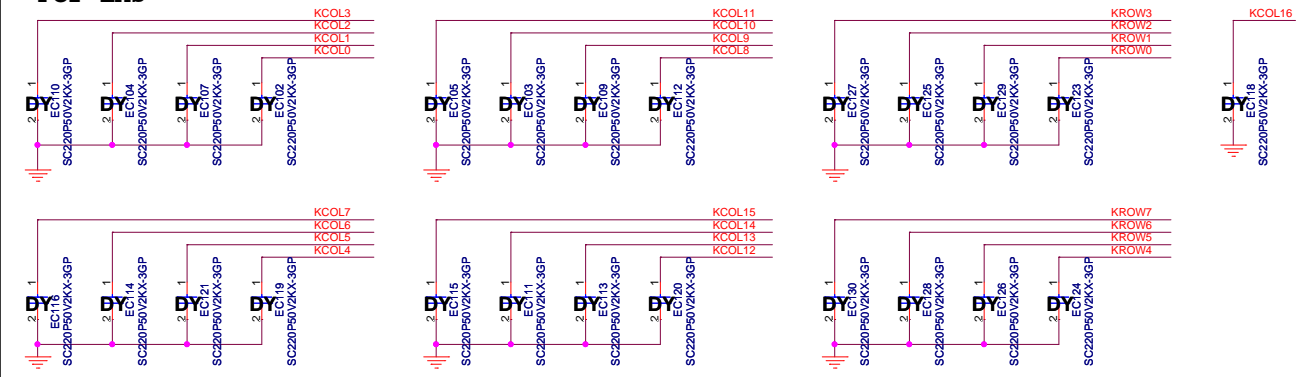


SSID = Touch.Pad

TouchPad Connector



For EMS

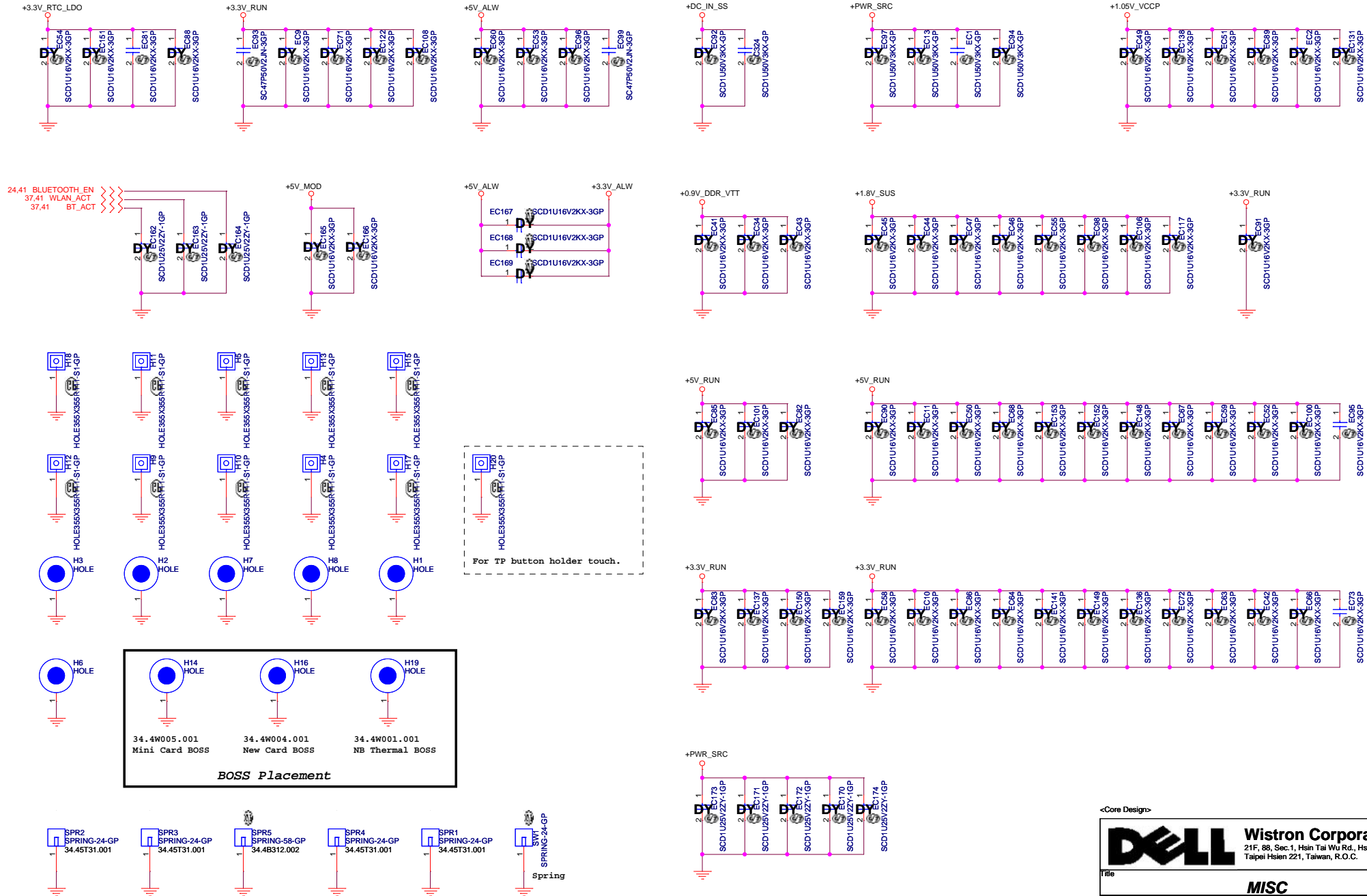


SSID = LOM

SSID = VIDEO

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| | | | |
|---|------------------------|---|-----------|
| <Core Design> | | | |
|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | | |
| LAN CONNECTOR / CRT | | | |
| Size | Document Number | | Rev |
| Custom | DR2 17" UMA | | SB |
| Date: | Monday, March 16, 2009 | Sheet | 46 of 58 |



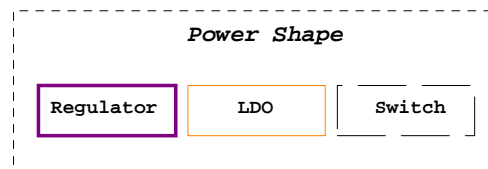
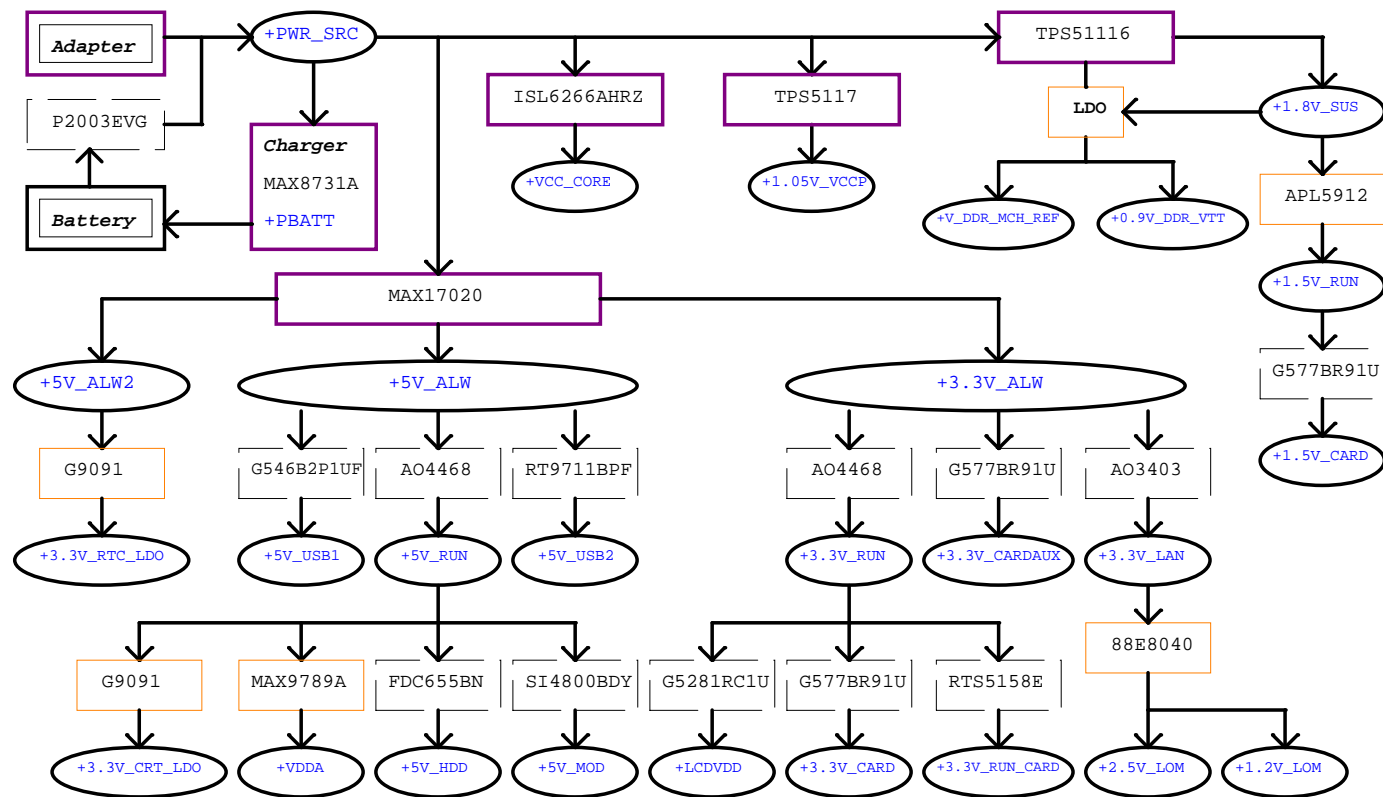
<Core Design>

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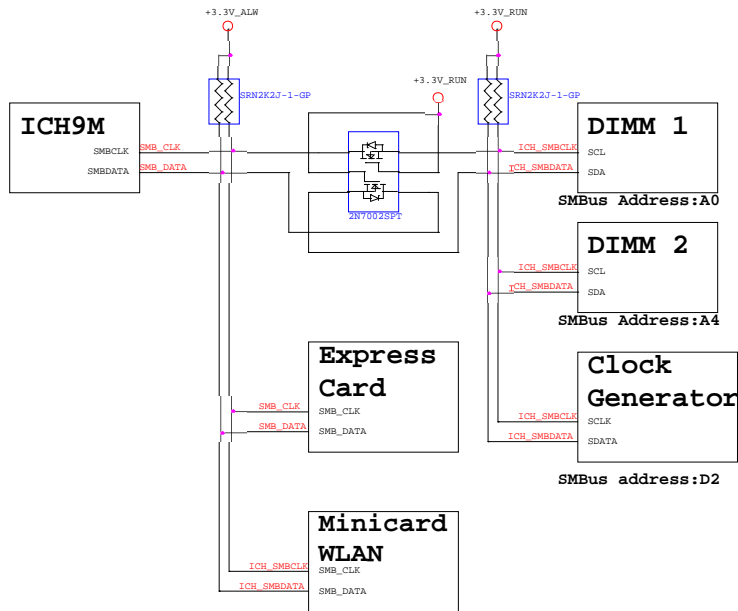
File

MISC

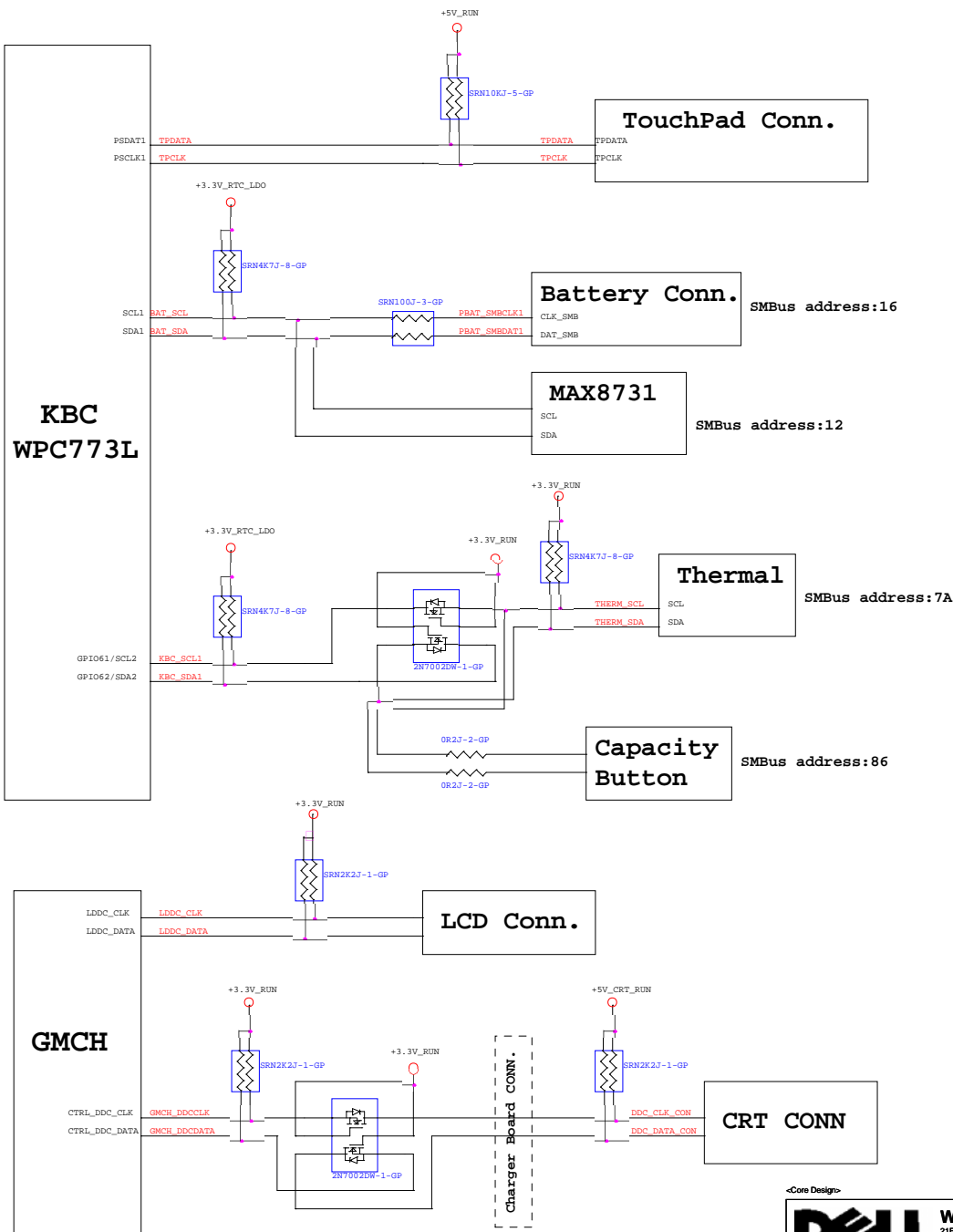
| Size | Document Number | Rev |
|--------|------------------------|----------------|
| Custom | DR2 17" UMA | SB |
| Date: | Monday, March 16, 2009 | Sheet 47 of 58 |



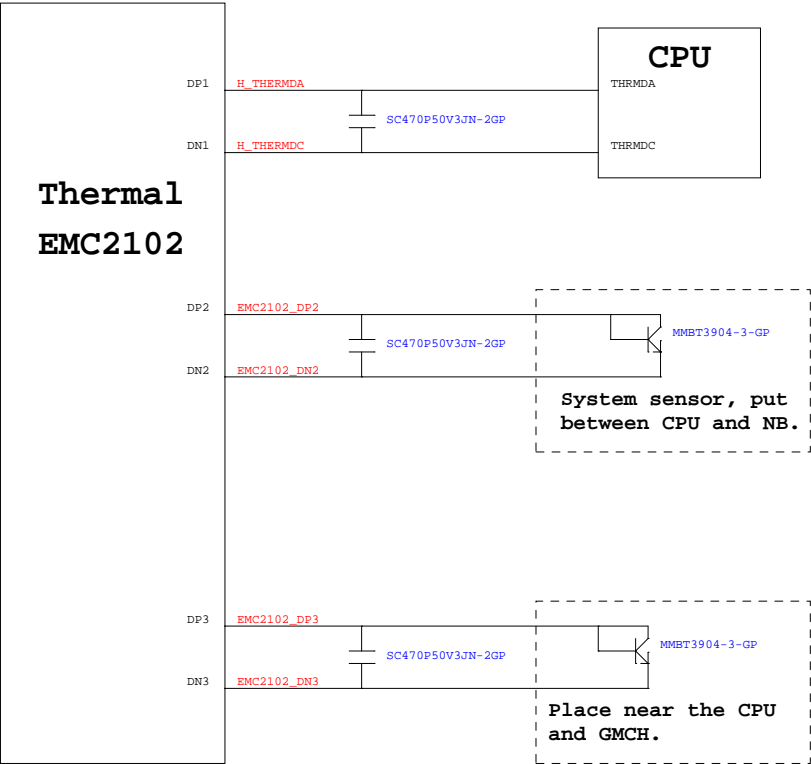
ICH9M SMBus Block Diagram



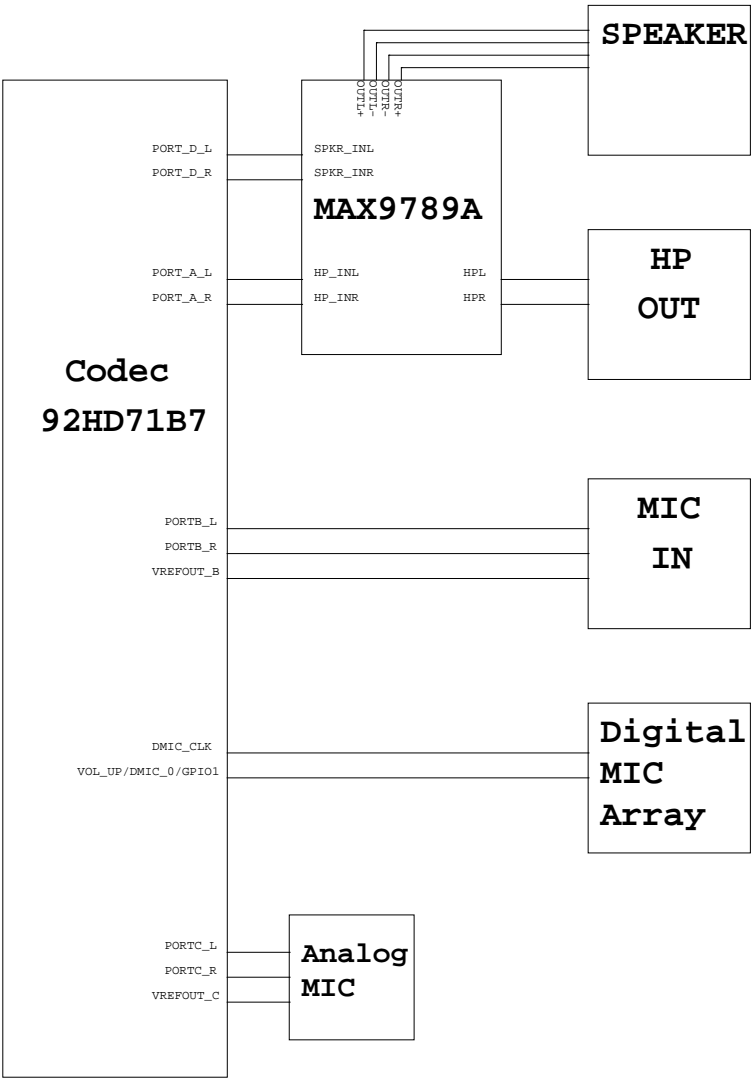
KBC SMBus Block Diagram



Thermal Block Diagram




Audio Block Diagram



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<Core Design>



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File

VGA-PCIE(1/4)

Size
Custom

Document Number
DR2 17" UMA


Rev
SB

Date: Monday, March 16, 2009

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<Core Design>



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File
VGA-VRAM(2/4)

Size
Custom


Document Number
DR2 17" UMA

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<Core Design>



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File
VGA-HDMI/STRAP(3/4)


Size
Custom

Document Number
DR2 17" UMA

Rev
SB


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| | | | |
|---|------------------------|---|-----------|
| <Core Design> | | | |
|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| File | | | |
| VGA-L VDS/TV/CRT/(4/4) | | | |
| Size | Document Number | | Rev |
| Custom | DR2 17" UMA | | SB |
| Date: | Monday, March 16, 2009 | Sheet | 54 of 58 |

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<Core Design>



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File

VRAM

Size
Custom

Document Number
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Date: Monday, March 16, 2009

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| DATE | VERSION | NO | PAGE | Modified List | Issue Description | OWNER |
|-------|---------|----|-------|--|--|-------|
| 06/03 | X01 | 1 | 45 | CN4 Pin.51 from +DC_IN change to GND. | CN4 Pin.51 should be ground. | EE |
| | | 2 | 24 | Dummy R422 | LID SW is push-pull type, no need pull high. | EE |
| | | 3 | 41 | CAMERA1 conn reduce from 10 to 8 pin. | Follow camera design. | EE |
| | | 4 | 42 | RTC1 CONN change p/n: 22.70031.001 to 62.70001.011. | Qty issue to change another. | EE |
| | | 5 | 46 | Exchange H14 and H6 names. | Correction. H14 for mini card boss ; H6 is hole. | EE |
| 06/05 | | 6 | 42 | Reverse LED1. | Correction. Amber for BAT_LED_B ; White for PWR_LED_B. | EE |
| | | 7 | 37,41 | Remove CN5 and related circuit in page.41. Add dummy R: R493, R494, R495, R496, R497, R498, R499 | Remove debug board connector. For debug mini card, change LPC Bus to mini card base. Set dummy res to avoid damaging MB or additional mini card. | EE |
| | | 8 | 37 | Dummy R210, R211 | For debug mini card. Set dummy res to avoid damaging MB or additional mini card. | EE |
| | | 9 | 24 | Dummy R150. Staff R151. | PCB Version for SB. | EE |
| 06/06 | | 10 | 42 | CN1 Pin.2 set to NC. Add R500 and dummy EC161. | Avoid shorting between KBC_PWRBTN# and GND. New R and C are for EMC pre-location. | EE |
| | | 11 | 24 | Dummy R406. Change R425, R422, R409, R406, R401, R404 to 100K ohm. | Dummy R406 for no keyboard detect function. R change to 100k for save power. | EE |
| 06/10 | | 12 | 36 | Update HDD symbol. | Update symbol and footprint for only SATA HDD. (no co-layout) | EE |
| | | 13 | 35-45 | Change All TP near connectors to AFTP (ZZ.AFT30.101). | For AFTE test pad. | EE |
| | | 14 | 04 | Change C461 and C462 from 15pF to 12pF. | For X3 cap choice by report suggestion. | EE |
| 06/12 | | 15 | 17 | Change C520 and C522 from 15pF to 12pF. | For X4 cap choice by report suggestion. | EE |
| | | 16 | 24,42 | Add 0 ohm R482 on EC_SPI_WP# and link to KBC/GPIO30. Change RN50 to 100k and Add R476 for EC_SPI_WP#. | KBC can control WP# of Flash ROM. R change to 100k for save power. | EE |
| | | 17 | 40 | Change L19 and L20 to 68.00082.531. | For EMI. | EE |
| | | 18 | 45 | Change M_RED to CN4 Pin.17 ; M_GREEN to CN4 Pin.21 ; M_BLUE to CN4 Pin.25. CN4 Pin.23 and Pin.27 to GND. | Avoiding noise to impact CRT signals. | EE |
| | | 19 | 47 | Add H20. | Add square GND for TP button holder touch. | EE |
| 06/16 | | 20 | 42 | Dummy CN2, R34. | Cap. button function is disable. | EE |
| | | 21 | 47 | Add dummy EC162, EC163, EC164. Add dummy EC165, EC166. Add dummy EC167, EC168, EC169. | For EMI. | EE |
| 06/17 | | 22 | 04 | Change R216 to 22 ohm. | The same clock dirve to U25 and U34. | EE |
| 06/18 | | 23 | 44 | Dummy EC110, EC104, EC107, EC102, EC105, EC103, EC109, EC112, EC127, EC125, EC129, EC123, EC118, EC116, EC114, EC121, EC119, EC115, EC111, EC113, EC120, EC130, EC128, EC126, EC124. | For EMI. | EE |
| 06/19 | | 24 | 43 | Short R26, R27. | No need 0 ohm R. | EE |
| | | 25 | 47 | Add SW1. | ME request. | EE |
| | | 26 | 35 | LCD1.38 link to GFX_PWR_SRC ; LCD1.37 set NC ; LCD1.35 link to +LCDVDD ; LCD1.34 link to +3.3V_RUN ; LCD1.33 link to LCD_BRIGHTNESS ; LCD1.32 to GND ; LCD1.31 link to LCD_CBL_DET#. | For LED backlight panel. | EE |
| | | 27 | 18 | Dummy R179, R423. | SW check vender ID by SMBus. | EE |
| | | 28 | 24 | Dummy R416, R418. | Cap. button function is disable. | EE |
| | | 29 | 40 | Change LOUT1 and MIC1 to 22.10133.D01. | Change jack source. | EE |
| | | 30 | 17,18 | Dummy U25.B10 link R506 to GND; U25.C18 link R501 to GND; Dummy U25.C21 link R502 to GND; U25.C11 link R503 to GND; Dummy U25.AE18 link R504 to GND; U25.AF21 link R505 to GND. Dummy R421, R424. | Avoiding abnormal action in U25(ICH9-M). | EE |
| | | 31 | 25 | Change R82 to 20K 1% ; Change R78 to 10K 1%. | For T8 shutdown is set 88 deg-C. | EE |
| 06/23 | | 32 | 47 | Add dummy EC170, EC171, EC172, EC173, EC174. | For EMI. | EE |
| 06/27 | | 33 | 42 | Change U23 to 72.25X16.A01. | Better performance. | EE |

<Core Design>

| | | | |
|---|---------------------------------------|---|--|
|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| | | Title Change List - EE (1/2) | |
| Size A3 | Document Number DR2 17" UMA | Rev SB | |
| Date: Monday, March 16, 2009 | | Sheet 56 of 58 | |

| DATE | VERSION | NO | PAGE | Modified List | Issue Description | OWNER |
|-------|---------|----------|---|---|--|-------|
| 07/30 | X02 | 34 | 18 | Staff R421, R424. (PT build cut-in) | Avoiding always issue interrupt event. | EE |
| | | 35 | 23 | Dummy R290 ; Staff R291. (PT build cut-in) | Adjust audio amp. gain value. | EE |
| | | 36 | 20 | Add dummy R507. | Add RUN power for LAN. | EE |
| | | 37 | 21 | Short R253, R254. | No need 0 ohm R. | EE |
| | | 38 | 24 | Staff R138, R150 ; Dummy R141, R151. | PCB Version for SC. | EE |
| | | 39 | 35 | Add R508 ; Change R359 to 49.9k ohm. | For LCD power sequence. | EE |
| | | 40 | 22,23 | Move C535 (Change 0.033uF), R472 to page.23. Remove C536 (Change 0.033uF), C542. Add R484 to gnd ; Add C566 for AUD_SET, C567 for AUD_BIAS. C565 for 6040 only. | For PC beep. | EE |
| | | 41 | 36 | Material change: HDD1 | ME request. | EE |
| | | 42 | 37 | Material change: CARD1 | ME request. | EE |
| | | 43 | 47 | Material change: SPR4 | ME request. | EE |
| 44 | | 09 | Add TP271 for U52/ SDVO_CTRLDATA. | TP. | EE | |
| 08/06 | | 45 | 41 | Short R79, R80. | No need 0 ohm R. | EE |
| | | 46 | 04 | Symbol change: U54. | For clock generator co-layout. | EE |
| | | 47 | - | Change to close line: R204, R200, R356, R139, R152, R408, R394, R390, R403, R402, R96, R120, R378, R360, R140, R373, R97, R405, R155, R154, R262, R266, R439, R265, R226, R269, R174, R175, R183, R432, R433, R434, R430, R431, R437, R191, R177, R270, R188, R436, R452, R259, R282, R250, R249, R467, R153, R81, R77. | No need 0 ohm R. | EE |
| | | 48 | 24,32 | Move R182 to page.24. | Movement. | EE |
| | | 49 | 37 | Short R428, R426 ; Add DY L21. | Pre-location for Minicard USB trace. | EE |
| | | 50 | - | Short R139, R96 , R155, R154, R226, R174, R175, R432, R433. | No need 0 ohm R. | EE |
| 08/07 | | 51 | 19 | Staff C488. | For DMI. | EE |
| 08/11 | | 52 | 23 | Use 2.2uF C564 and C557 for Maxim U62 IC. | For improving bobo sound. | EE |
| 08/15 | | 53 | 32 | Material change: TC23. (DY) | Material issue. | EE |
| | 54 | 11 | Material change: TC19, TC21. | Material issue. | EE | |
| 09/02 | A00 | 55 | 21 | USB_PP10 for U34.5 ; USB_PN10 for U34.4. (ST build cut-in) | Schematic modification. | EE |
| | | 56 | 24 | Staff R151 ; Dummy R150. | PCB Version for -1(Xbuild). | EE |
| 57 | | 24 | Add dummy R509 to gnd for KBC GPIO24. (09/10 update) | For GM45. | EE | |
| 58 | | 05,17 | Dummy R76 ; Staff R167 | For H_THRMTRIP# to SB. | EE | |
| 59 | | 12,20,24 | Change to close line: R115, R246, R182, R158, R159, R170. | No need 0 ohm R. | EE | |
| 60 | | 37 | Remove L21. | No need L21. | EE | |
| 09/09 | | 61 | 19 | Staff R453, C511 ; DY C521. | Follow Intel DG 2.0. | EE |
| 09/10 | | 62 | 04 | Short RN42, RN43, RN44, RN45, RN48, RN22, RN23, RN54, RN53, RN52, RN51. | No need 0 ohm R. | EE |
| 09/22 | | 63 | 21 | Add dummy R510 and C568. Staff R282 0 ohm. | For U34 power bounce issue. | EE |
| | | 64 | 04 | Dummy R196. | For debug. Normally, no need it. | EE |
| | | 65 | 25 | R82 change to 10k ; R78 change to 2.37k. | For T8 thermal shutdown setting. | EE |
| 10/02 | | 66 | 23 | Staff R288 ; Dummy R289. | For Audio amp. gain. | EE |
| | 67 | 21 | Dummy R284, C318. Staff R282 to Bead 68.00082.531. Staff R510 to 2.2K ; Staff C568. | For U34 power bounce issue. | EE | |
| | | | | | | |

<Core Design>

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| | | Title: Change List - EE (2/2) | |
| Size A3 | Document Number DR2 17" UMA | Rev SB | |
| Date: Monday, March 16, 2009 | | Sheet 57 of 58 | |

| DATE | VERSION | NO | PAGE | Modified List | Issue Description | OWNER |
|-------|---------|----------------------|-------------|---|--|----------|
| 06/03 | X01 | 1 | 32 | R189 change to 2.2K ohm, C216 dummy. | For +1.5V_RUN sequence. | Power EE |
| | | 2 | 30 | C378 change to 0.01uF. | For +1.05V_VCCP sequence. | Power EE |
| | | 3 | 34 | C316 change from 4.7nF to 0.01uF. | For +3.3V_RUN sequence and improve +3.3V_ALW voltage drop due to SW(U31) turn on quickly (higher loading). | Power EE |
| | | 4 | 34 | Staff C314 and change from 4.7nF to 6.8nF. | For +5V_RUN sequence and improve +5V_ALW voltage drop due to SW(U30) turn on quickly (higher loading). | Power EE |
| 06/05 | | 5 | 36 | Dummy Q20, U57, R462, R457, C527 and U58, U28, R251, R252, C293, C295 Change R258, R256 to G81, G82 Change R278, R279, R277, R276 to G83, G84, G85, G86 | No sniffer function, no control HDD & ODD power. | Power EE |
| 06/06 | | 6 | 27 | R136 change to 270k and R108 change to 237k | For 5V/3.3V OCP | Power EE |
| | | 7 | 28 | R38 change to 12.1k R323 change to 3.92k , C360 change to 0.047 uF 10V X7R | R38 for VCORE OCP R323 and C360 for transient and load line. | Power EE |
| | | 8 | 31 | PC9 to GND. | PC9 to GND otherwise DC-DC IC can not obtain power to generate 1.8V/0.9V output. | Power EE |
| | | 9 | 31 | PR2 change to 9.31k ohm. | For 1.8V OCP. | Power EE |
| 06/10 | | 10 | 30 | Add D23. | For power sequence. | Power EE |
| 06/18 | | 11 | 18,24 | Remove U60, R482, R476 and change trace name VRMPWRGD to VGATE_PWRGD. | For power sequence. | Power EE |
| 06/23 | | 12 | 31 | PR7.1 link to +5116_PWR_SRC. | Reserve for other source. | Power EE |
| | | 13 | 30 | Rename "+1.05V_SUSP" to "+1.05V_RUNP" | Correct naming. | Power EE |
| 06/23 | | 14 | 26,45 | Material change: U37, U46, U47. | NIKO-SEM P2003EVG component has some risk. | Power EE |
| 07/30 | X02 | 15 | 31 | Change PR7 value from 622k to 619k ohm. | For 2nd source. | Power EE |
| 08/11 | | 16 | 26,45 | Material change: U37, U46, U47. | Power team request. | Power EE |
| 09/03 | A00 | 17 | 26,27,28,31 | Change to close line: R46 ,R137 ,R127,R106 ,R384 ,R391 ,R35 ,R29 ,R307 ,R308 ,R309 ,R303 ,R304 , R298 ,R301 ,R310 ,R313 ,PR14. | No need 0 ohm R. | Power EE |
| | | 18 | 26 | R61 change 4.7k to 10k. | Power team request. | Power EE |
| XX | | 19 20 21 22 | | | | |
| XX | | | | | | |
| | | | | | | |
| | | | | | | |
| XX | | 23 | x | x | x | Power EE |
| XX | | 24 | x | x | x | Power EE |
| | 25 | x | x | x | Power EE | |